6437 102179

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/24/03 Serial # 09/854,269 Priority Application Date 9/18/97

Your Name M. Lewis Examiner # _____

AU 2829 Phone 305-3743 Room Plaza 3-3809

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

08-25-03 A10:42 IN

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-9 (1 & 4 independent)

Problems: See Paragraphs 3 & 4-8

Solution " " 15, 16 & abstract

an additional search to Also please focus on the specific composition of the solder (See Claims 7 & 8)

Staff Use Only		Type of Search		Vendors	
Searcher:	HARRISON	Structure (#)		STN	X
Searcher Phone:	306-5429	Bibliographic	X	Dialog	X
Searcher Location:	STIC-EIC2800, CP4-9C18	Litigation		Questel/Orbit	
Date Searcher Picked Up:	9-2-03	Fulltext	X	Lexis-Nexis	
Date Completed:	9-2-03	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	60	Other		Other	
Online Time:	80				

STIC Search Report
EIC 2800

STIC Database Tracking Number: 102179

TO: Monica Lewis **Location: CP3-3B07** **Art Unit: 2822** **9/3/2003** **Case Serial Number: 09/854,269**	**From: Jeff Harrison** **Location: STIC-EIC2800** **CP4-9C18** **Phone: 306-5429** **Email: harrison, jeff**

Search Notes

Examiner Lewis,

Re -- thermal expansion / elongated / solder column interconnects / / dielectric sheet / Sn-Pb-Cu composite solders

with a 9/18/1997 priority date to beat.

Attached are search results from the patent and NPL literature (Chemical Abstracts, INSPEC, DWPI, JAPIO, fulltext EPO/WO/PCT.)

Based on this, if you have questions or would like a refocused search, please contact me.

Thanks,
Jeff

Jeff Harrison
Team Leader, STIC-EIC2800
CP4-9C18, 703-306-5429

FILE 'INPADOC, WPIX, JAPIO, HCAPLUS' ENTERED AT 14:39:28 ON 02 SEP 2003
L1 3 S US2001020748/PN
L2 SEL PLU=ON L1 1- IC RN : 1 TERM
L3 13699 S L2
L4 3 S L1 AND L3
L5 SEL PLU=ON L4 1- IC : 1 TERM
L6 SEL PLU=ON L4 1- IC MC : 4 TERMS
L7 22824 S L6
L8 100 S L7 AND (LONG##### OR ELONGAT#####)(6A)(SOLDER#### OR INTERCONNECT##### OR CONNECT#####)
L9 22824 S L6
L10 123 S L9 AND (LONG##### OR ELONGAT##### OR DISTAL####)(6A)(SOLDER#### OR INTERCONNECT##### OR CONNECT##### OR TERMINA######)
L11 22824 S L6
L12 89 S L11 AND COMPLIAN#####
L13 22824 S L6
L14 113 S L13 AND FATIGUE
L15 22824 S L6
L16 170 S L15 AND FAILURE
L17 22824 S L6
L18 75 S L17 AND (DECOUPL###### OR UNCOUPL#####)
L19 22824 S L6
L20 22824 S L6
L21 916 S L20 AND ((TEMPERATURE OR HEAT OR TEMP OR HEATING OR THERMAL####)(2A)(STRESS#### OR STRAIN#### OR CYCL#### OR EXPAN######) OR CTE)
L22 22824 S L6
L23 50 S L22 AND FLEX#########(3A)(SOLDER#### OR LONG#### OR ELONG#####)
L24 113852 S CTE OR (DIFFEREN######(4A) THERMAL#####
AND THERMAL###(2A) EXPAN#######) OR THERMAL EXPANSION
L25 203 S SOLDER COLUMN
L26 32661 S SOLDER######(10A)(CONTACT#### OR PAD) OR CONTACT PAD
L27 8135 S COLUMN####(2A) INCLU#######
L28 107 S SOLDER MASS
L29 52862 S LEAD(1A) TIN OR SN(1A) PB OR PBSN OR SNPB
L30 21386 S L29 AND (CU OR COPPER)
L31 15 S PBSNCU OR SNPBCU OR SNCUPB OR PBCUSN OR CUPBSN OR CUSNPB
L32 4450 S L24 AND SOLDER#######
L33 1757 S L32 AND (PACKAG###### OR INTERCONNECT##### OR CHIP)
L34 1 S (L8 OR L10) AND L33
L35 30 S ELONGAT###### AND L8
L36 33 S ELONGAT###### AND L10
L37 4 S ELONGAT###### AND L12
L38 6 S ELONGAT###### AND L14
L39 2 S ELONGAT###### AND L16
L40 1 S ELONGAT###### AND L18
L41 16 S ELONGAT###### AND L21
L42 7 S ELONGAT###### AND L23
L43 5638 S ELONGAT###### AND L24
L44 10 S ELONGAT###### AND L25
L45 630 S ELONGAT###### AND L26
L46 189 S ELONGAT###### AND L27
L47 14 S ELONGAT###### AND L28
L48 661 S ELONGAT###### AND (L29 OR L30)
L49 2 S L31 AND SOLDER#####
L50 0 S L31 AND (PACKAG###### OR INTERCONNECT##### OR CHIP)
L51 12 S L43 AND L45
L52 0 S L43 AND L46
L53 18 S L43 AND L48
L54 11 S L45 AND L48
L55 2 S L45 AND L46
L56 100 S L8 AND L10
L57 0 S L8 AND L12
L58 6 S L8 AND L14
L59 3 S L8 AND L16
L60 0 S L8 AND L18
L61 7 S L8 AND L21
L62 1 S L8 AND L23
L63 6 S L8 AND L24
L64 2 S L8 AND L25
L65 15 S L8 AND L26
L66 1 S L8 AND L27
L67 3 S L8 AND L28
L68 6 S L8 AND (L29 OR L30)
L69 7 S L12 AND L14

FILE 'INPADOC, WPIX, JAPIO, HCAPLUS' ENTERED AT 14:39:28 ON 02 SEP 2003
L70 2 S L18 AND L21
L71 87 S L24 AND (L25 OR L28 OR L18 OR L16 OR L14 OR L12 OR L10)
L72 87 S L71 AND (CTE OR EXPAN########)
L73 23 S L72 AND (FLEX######## OR ELONG########)

FILE 'REGISTRY' ENTERED AT 15:03:20 ON 02 SEP 2003
L74 399 S CU.PB.SN/MF
L75 616 S PB.SN/MF
L76 11 S LEAD TIN AND PB/ELS,MAC AND SN/MAC
L77 4578 S PB/MAC AND SN/MAC AND CU/MAC
L78 1820 S L77 AND LEAD ALLOY
L79 1901 S L77 AND TIN ALLOY
L80 2406 S (L78 OR L79)
L81 2338 S L80 NOT O/ELS,MAC

FILE 'HCAPLUS' ENTERED AT 15:05:42 ON 02 SEP 2003
L82 46 S L74(L)SOLDER#####
L83 2381 S L75(L)SOLDER#####
L84 944 S L76(L)SOLDER#####
L85 1858 S L81(L)SOLDER#####
L86 2837 S (L82 OR L83 OR L84 OR L85)
L87 29 S L86 AND ELONG##########
L88 1487 S L5
L89 1487 S L5
L90 11 S L86 AND L89
L91 0 S L18 AND L23
L92 11 S L82 AND (PACKAG###### OR CHIP##### OR DISTAL## OR INTERCONNECT##### OR TERMINA##### OR FLEX#####)
L93 51 S L87 OR L90 OR L92
L94 22 S L93 AND P/DT
L95 29 S L93 NOT L94
L96 12 S L95 AND PY>1997
L97 17 S L95 NOT L96
L98 14 S L94 AND PRY>1997
L99 2 S L98 AND 1997/PRY
L100 8 S L94 NOT L98
L101 27 S L97 OR (L99 OR L100)
L102 SEL PLU=ON L101 1- PRN : 19 TERMS

FILE 'INPADOC, WPIX, JAPIO, HCAPLUS' ENTERED AT 15:12:56 ON 02 SEP 2003
L103 65 S L102
L104 173 S (L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41 OR L42) OR L44 OR L47 OR (L49 OR L50 OR L51 OR L52 OR L53 OR L54 OR L55) OR (L58 OR L59 OR L60 OR L61 OR L62 OR L63 OR L64 OR L65 OR L66 OR L67 OR L68 OR L69 OR L70) OR L73
L105 173 S L104 NOT L103
L106 155 S L105 AND P/DT
L107 18 S L105 NOT L106
L108 4 S L107 AND PY>1997
L109 14 S L107 NOT L108
L110 80 S L106 AND PRY>1997
L111 75 S L106 NOT L110
L112 28 S L106 AND PRY=1997
L113 95 S (L111 OR L112)
L114 3 S L113 AND INCLUS######
L115 19 S L113 AND COLUMN######
L116 0 S L113 AND PRECIP#######
L117 70 S L113 AND SOLDER#######
L118 58 S L113 AND ELONG########
L119 16 S (L29 OR L30 OR L31) AND L113
L120 86 S (L114 OR L115 OR L116 OR L117 OR L118 OR L119)
L121 9 S L113 NOT L120
L122 61 S L120 AND (MICROELECTRONIC#### OR PACKAG#### OR ELONGAT##### OR SOLDER##### OR INTERCONNECT######)/TI
L123 10 S L120 AND TESSERA?/CS,PA
L124 53 S L122 NOT L123

02sep03 14:26:32 User259284 Session D2364.1

File 2:INSPEC 1969-2003/Aug W4

*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

Set	Items	Description
S1	0	CI=(CU DOP(S)PB SS(S)SN SS)(S)NE=3
S2	0	CI=(CU DOP(S)PB BIN(S)SN BIN)(S)NE=3
S3	49	CI=(CU SS(S)PB SS(S)SN SS)(S)NE=3
S4	20	S3 AND SOLDER????????
S5	23745	R1:R2 OR R11 OR CTE OR THERMAL()EXPANSION????
S6	882	SOLDER????? AND S5
S7	6	S6 AND ELONG????????? AND S6
S8	62	S6 AND FLEX??????????
S9	18	S8 AND INTERCONNECT????????
S10	0	S8 AND TERMINA????????
S11	18	S9 NOT S7

02sep03 14:31:40 User259284 Session D2364.3

SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2003/Aug W04
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030828,UT=20030821
(c) 2003 WIPO/Univentio

Set	Items	Description
S1	12256	DISTAL????/TI,AB
S2	2092	(FACING OR FACE??)(W)AWAY/TI,AB
S3	155	S1:S2 AND SOLDER??????/TI,AB,CM
S4	51	S3 AND ELONGAT?????????/TI,AB,CM
S5	2	S4 AND DIELECTRIC????/TI,AB,CM
S6	0	S4 AND (THERMAL????. OR CTE)/TI,AB
S7	7	S4 AND (THERMAL???? OR CTE)/TI,AB,CM
S8	9	S5 OR S7

L124 ANSWER 52 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:659784 HCAPLUS
DN 133:246153
TI Semiconductor flip-chip **package** and method for the fabrication thereof
IN Capote, Miguel A.; Zhou, Zhiming; Zhu, Xiaoqi; Zhou, Ligui
PA USA
SO U.S., 22 pp.
CODEN: USXXAM
DT **Patent**
LA English
IC ICM H01L023-48
ICS H01L023-52; H01L029-40
NCL 257783000
CC 76-3 (Electric Phenomena)
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6121689	A	20000919	US 1998-120172	19980721 <--
	US 6297560	B1	20011002	US 1998-137971	19980821 <--
	US 6335571	B1	20020101	US 2000-517839	20000302 <--
	US 6518677	B1	20030211	US 2000-662641	20000915 <--
	US 6566234	B1	20030520	US 2000-662642	20000915 <--
	US 2002031868	A1	20020314	US 2001-948921	20010907
	US 6399426	B2	20020604		
PRAI	US 1997-53407P	P	19970721 <--		
	US 1997-56043P	P	19970902 <--		

AB A simplified process for flip-chip attachment of a chip to a substrate is provided by pre-coating the chip with an encapsulant underfill material having sep. discrete **solder columns** therein to eliminate the conventional capillary flow underfill process. Such a structure permits incorporation of remeltable layers for rework, test, or repair. It also allows incorporation of elec. redistribution layers. In one aspect, the chip and pre-coated encapsulant are placed at an angle to the substrate and brought into contact with the pre-coated substrate, then the chip and pre-coated encapsulant are pivoted about the 1st point of contact, expelling any gas therebetween until the **solder** bumps on the chip are fully in contact with the substrate. There is also provided a flip-chip configuration having a complaint **solder/flexible** encapsulant understructure that deforms generally laterally with the substrate as the substrate undergoes **expansion** or contraction. With this configuration, the complaint **solder/flexible** encapsulant understructure absorbs the strain caused by the **difference** in the **thermal** coeffs. of **expansion** between the chip and the substrate without bending the chip and substrate.

IT Coating process
Encapsulation
Semiconductor device fabrication
(semiconductor flip-chip package and method for the fabrication thereof)

L124 ANSWER 1 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 207535975 INPADOC ED 20030624 EW 200325 UP 20030722 UW 200329
TI SEMICONDUCTOR FLIP-CHIP **PACKAGE** AND METHOD FOR THE FABRICATION THEREOF
IN CAPOTE MIGUEL A.; ZHOU ZHIMING; ZHU XIAOQI; ZHOU LIGUI
INS CAPOTE MIGUEL A; ZHOU ZHIMING; ZHU XIAOQI; ZHOU LIGUI
INA US; US; US; US
PA AGUILA TECHNOLOGIES, INC.
PAS AGUILA TECHNOLOGIES INC
PAA US
DT **Patent**
PIT USBA PATENT (NO PREVIOUS PRE-GRANT PUBLICATION)
PI US 6566234 BA 20030520
AI US 2000-662642 A 20000915
PRAI **US 2000-662642 A 20000915**
US 1998-120172 A3 19980721
US 1997-56043P P 19970902
US 1997-53407P P 19970721
AIT USA patent application
PRAIT USA patent application
USA3 appl. number is cited as basic appl. number from which a division was made
USP provisional application for patent
RLI US now patented
ICM (7) H01L021-30
ICS (7) H01L021-46
EPC H01L21/56F; H01L21/60C4; H01L23/498E
NCL 438458; X438464; X438460
AB A simplified process for flip-chip attachment of a chip to a substrate is provided by pre-coating the chip with an encapsulant underfill material having separate discrete **solder columns** therein to eliminate the conventional capillary flow underfill process. Such a structure permits incorporation of remeltable layers for rework, test, or repair. It also allows incorporation of electrical redistribution layers. In one aspect, the chip and pre-coated encapsulant are placed at an angle to the substrate and brought into contact with the pre-coated substrate, then the chip and pre-coated encapsulant are pivoted about the first point of contact, expelling any gas therebetween until the **solder** bumps on the chip are fully in contact with the substrate. There is also provided a flip-chip configuration having a complaint **solder/flexible** encapsulant understructure that deforms generally laterally with the substrate as the substrate undergoes **expansion** or contraction. With this configuration, the complaint **solder/flexible** encapsulant understructure absorbs the strain caused by the **difference** in the **thermal** coefficients of **expansion** between the chip and the substrate without bending the chip and substrate.

7/21/97 priority

L124 ANSWER 4 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 168254023 INPADOC ED 20020226 EW 200208 UP 20030317 UW 200311
TI SEMICONDUCTOR FLIP-CHIP **PACKAGE** AND METHOD FOR THE FABRICATION THEREOF
IN CAPOTE MIGUEL A.; ZHU XIAOQI
INS CAPOTE MIGUEL A; ZHU XIAOQI
INA US; US
PA CAPOTE MIGUEL A.; ZHU XIAOQI
PAS CAPOTE MIGUEL A; ZHU XIAOQI
PAA US; US
DT **Patent**
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2002014703 AA 20020207
AI US 2001-935432 A 20010820
PRAI **US 2001-935432 A 20010820**
US 1998-137971 A3 19980821
US 1997-56043P P 19970902
US 1997-53407P P 19970721
AIT USA patent application
PRAIT USA patent application
USA3 appl. number is cited as basic appl. number from which a division was made
USP provisional application for patent
RLI US now patented
ICM (7) H01L021-44
ICS (7) H01L021-48; (7) H01L021-50; (7) H01L023-48
EPC H01L21/56F; H01L21/60C4
NCL 257778; X438107
AB A simplified process for flip-chip attachment of a chip to a substrate is provided by pre-coating the chip with an encapsulant underfill material having separate discrete **solder columns** therein to eliminate the conventional capillary flow underfill process. There is also provided a flip-chip configuration having a **flexible** tape lamination for underfill encapsulation. With this configuration, the complaint **solder/flexible** encapsulant understructure absorbs the strain caused by the **difference** in the **thermal** coefficients of **expansion** between the chip and the substrate and provides enhanced ruggedness.

L124 ANSWER 6 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 136657943 INPADOC ED 20001011 EW 200040 UP 20030317 UW 200311
TI SEMICONDUCTOR FLIP-CHIP **PACKAGE** AND METHOD FOR THE FABRICATION THEREOF
IN CAPOTE, MIGUEL A.; ZHOU, ZHIMING; ZHU, XIAOQI; ZHOU, LIGUI
INS CAPOTE MIGUEL A; ZHOU ZHIMING; ZHU XIAOQI; ZHOU LIGUI
INA US; US; US; US
PA MIGUEL ALBERT CAPOTE
PAS MIGUEL ALBERT CAPOTE
PAA US
DT **Patent**
PIT USA UNITED STATES PATENT
PI US 6121689 A 20000919
AI US 1998-120172 A 19980721
PRAI **US 1998-120172 A 19980721**
US 1997-56043P P 19970902
US 1997-53407P P 19970721
AIT USA patent application
PRAIT USA patent application
USP provisional application for patent
OSCA 133:246153
ICM (7) H01L023-48
ICS (7) H01L023-52; (7) H01L029-40
EPC H01L21/56F; H01L21/60C4
NCL 257783; X257773; X257787; X257778
AB A simplified process for flip-chip attachment of a chip to a substrate is provided by pre-coating the chip with an encapsulant underfill material having separate discrete **solder columns** therein to eliminate the conventional capillary flow underfill process. Such a structure permits incorporation of remeltable layers for rework, test, or repair. It also allows incorporation of electrical redistribution layers. In one aspect, the chip and pre-coated encapsulant are placed at an angle to the substrate and brought into contact with the pre-coated substrate, then the chip and pre-coated encapsulant are pivoted about the first point of contact, expelling any gas therebetween until the **solder** bumps on the chip are fully in contact with the substrate. There is also provided a flip-chip configuration having a complaint **solder/flexible** encapsulant understructure that deforms generally laterally with the substrate as the substrate undergoes **expansion** or contraction. With this configuration, the complaint **solder/flexible** encapsulant understructure absorbs the strain caused by the **difference** in the **thermal** coefficients of **expansion** between the chip and the substrate without bending the chip and substrate.

L124 ANSWER 2 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 198312695 INPADOC ED 20030303 EW 200309 UP 20030317 UW 200311
TI SEMICONDUCTOR FLIP-CHIP **PACKAGE** AND METHOD FOR THE FABRICATION THEREOF
IN CAPOTE MIGUEL A.; ZHOU ZHIMING; ZHU XIAOQI; ZHOU LIGUI
INS CAPOTE MIGUEL A; ZHOU ZHIMING; ZHU XIAOQI; ZHOU LIGUI
INA US; US; US; US
PA CAPOTE MIGUEL ALBERT
PAS CAPOTE MIGUEL ALBERT
PAA US
DT **Patent**
PIT USBA PATENT (NO PREVIOUS PRE-GRANT PUBLICATION)
PI US 6518677 BA 20030211
AI US 2000-662641 A 20000915
PRAI **US 2000-662641 A 20000915**
US 1998-120172 A1 19980721
US 1997-53407P P 19970721
US 1997-56043P P 19970902
AIT USA patent application
PRAIT USA patent application
USA1 appl. number is cited as basic appl. number for a continuation
USP provisional application for patent
RLI US now patented
ICM (7) H01L023-48
EPC H01L21/56F; H01L21/60C4; H01L23/498E
NCL 257783; X257778; X257787; X257792
AB A simplified process for flip-chip attachment of a chip to a substrate is provided by pre-coating the chip with an encapsulant underfill material having separate discrete **solder columns** therein to eliminate the conventional capillary flow underfill process. Such a structure permits incorporation of remeltable layers for rework, test, or repair. It also allows incorporation of electrical redistribution layers. In one aspect, the chip and pre-coated encapsulant are placed at an angle to the substrate and brought into contact with the pre-coated substrate, then the chip and pre-coated encapsulant are pivoted about the first point of contact, expelling any gas therebetween until the **solder** bumps on the chip are fully in contact with the substrate. There is also provided a flip-chip configuration having a complaint **solder/flexible** encapsulant understructure that deforms generally laterally with the substrate as the substrate undergoes **expansion** or contraction. With this configuration, the complaint **solder/flexible** encapsulant understructure absorbs the strain caused by the **difference** in the **thermal** coefficients of **expansion** between the chip and the substrate without bending the chip and substrate.

LEGAL STATUS

7/21/97 priority

L123 ANSWER 6 OF 10 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2001-601801 [68] WPIX
CR 1996-097761 [10]; 1997-203137 [18]; 1997-203234 [18]; 1998-007997 [01];
DNN N2001-448997 DNC C2001-178254
TI Microelectronic assembly fabrication involves juxtaposing sheet with microelectronic element, attaching tip ends of sheet to contacts of element, and separating sheet and element to form leads.
DC A85 L03 U11
IN FJELSTAD, J; SMITH, J W
PA (FJEL-I) FJELSTAD J; (SMIT-I) SMITH J W; (TESS-N) **TESSERA INC**
CYC 1
PI US 2001010400 A1 20010802 (200168)* 19p H01L023-48
US 6486547 B2 20021126 (200303) H01L023-48
ADT US 2001010400 A1 Provisional US 1995-3927P 19950918, CIP of US 1996-715571 19960918, Provisional US 1997-56965P 19970826, Provisional US 1997-57741P 19970828, Div ex US 1998-140589 19980826, US 2001-798809 20010302; US 6486547 B2 Provisional US 1995-3927P 19950918, CIP of US 1996-715571 19960918, Provisional US 1997-56965P 19970826, Provisional US 1997-57741P 19970828, Div ex US 1998-140589 19980826, US 2001-798809 20010302
FDT US 2001010400 A1 Div ex US 6228686; US 6486547 B2 Div ex US 6228686, CIP of US 6329607
PRAI US 2001-798809 20010302; US 1995-3927P 19950918; US 1996-715571 19960918; **US 1997-56965P 19970826**; **US 1997-57741P 19970828**; US 1998-140589 19980826
IC ICM H01L023-48
ICS **H01L023-52**; H01L029-40
AB US2001010400 A UPAB: 20030710
NOVELTY - A component for a microelectronic assembly comprises a sheet (10), e.g. of polymeric dielectric material having **elongated** lead regions (24) partially separated from the main region (26) of the sheet by gaps (22) in the sheet, and having conductors (extending along the lead regions. The lead regions are connected to contacts on the microelectronic element which is moved away from the main region of the sheet to bend the lead regions downwards to form leads projecting form the main region of the sheet.

DETAILED DESCRIPTION - The sheet includes a main region and gaps partially surrounding and define a set of **flexible elongated** lead regions of the sheet. Each lead region has a fixed end connected to the main region and a tip end remote from the fixed end. The sheet includes a continuous layer of polymeric material with top and bottom surfaces extending within the main region and the lead regions, the lead regions of the sheet including metallic conductors extending on the polymeric layer between the tip ends (28) and the fixed ends (30) of the lead regions. At least some of the conductors are electrically isolated from others of the conductors. Terminals (34) are placed on the main region (26) and are electrically connected to at least some of the metallic conductors.

Preferred component: A metallic potential plane overlies the surface of the sheet in the main region, at least some of the metal conductors being electrically isolated from the potential plane.

The metallic conductors are formed on either one or both surfaces of the sheet and the potential plane is formed over the conductors.

USE - For making microelectronic assemblies.

ADVANTAGE - The sheet is manufactured in a few inexpensive steps and the formed leads incorporate polymeric portions which physically reinforce the metallic conductors and permit the use of thin metallic conductors. The **fatigue** resistance of the leads is enhanced.

DESCRIPTION OF DRAWING(S) - The drawing shows a bottom plan view of a component.

Flexible dielectric material 10
Bottom surface 12
Gaps 22
Lead regions 24
Main region 26
Tip end of lead regions 28
Fixed end of lead regions 30
Metal conductive strip 32

8/26/97 priority

Terminals 34
Bonding material masses 36
Vias 38
Dwg.1/15
FS CPI EPI
FA AB; GI
MC CPI: A99-A; L04-C24A

L124 ANSWER 3 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 189031351 INPADOC ED 20021129 EW 200247 UP 20030616 UW 200324
TI RAISED CONTACT STRUCTURES (**SOLDER COLUMNS**)
IN KHANDROS IGOR Y.; MATHIEU GAETAN L.
INS KHANDROS IGOR Y; MATHIEU GAETAN L
INA US; US
PA FORMFACTOR, INC.
PAS FORMFACTOR INC
PAA US
DT **Patent**
PIT USBA PATENT (NO PREVIOUS PRE-GRANT PUBLICATION)
PI US 6476333 BA 20021105
AI US 1996-735817 A 19961021
PRAI US 1996-735817 A 19961021
US 1994-340144 A1 19941115
US 1993-152812 A2 19931116
AIT USA patent application
PRAIT USA patent application
USA1 appl. number is cited as basic appl. number for a continuation
USA2 appl. number is cited as basic appl. number for a continuation in part
RLI US 5476211 now patented
ICM (7) H01R012-04
EPC G01R1/073B2; H01L23/485B; H01L23/49; H01L23/498C; H01L25/065M; H01L25/16; H05K3/30D2; H05K3/32C2; H05K3/34C3B; H05K3/40B1; G01R1/073B4; G01R31/316F; H01L21/00S2V; H01L21/00S2R; H01L21/48C4C; H01L21/56F; H01L21/60B2; H01L21/60C; H01L21/60C4B; H01L21/60C4; H01L21/66P; H01L23/48F
NCL 174267
AB An interconnection contact structure assembly including an electronic component having a surface and a conductive contact carried by the electronic component and accessible at the surface. The contact structure includes an internal flexible **elongate** member having first and second ends and with the first end forming a first intimate bond to the surface of said conductive contact terminal without the use of a separate bonding material. An electrically conductive shell is provided and is formed of at least one layer of a conductive material enveloping the **elongate** member and forming a second intimate bond with at least a portion of the conductive contact terminal immediately adjacent the first intimate bond.

1996 priority

L124 ANSWER 5 OF 53 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 163368822 INPADOC ED 20011211 EW 200149 UP 20011211 UW 200149
TI **MICROELECTRONIC PACKAGE** AND METHOD OF FORMING THE SAME
IN RINNE, GLENN A.; DEANE, PHILIP A.
INS RINNE GLENN A; DEANE PHILIP A
INA US; US
PA MCNC
PAS MCNC
PAA US
TL English
DT **Patent**
PIT TWB PATENT
PI TW 440982 B 20010616
AI TW 1997-107544 A 19970602
PRAI US 1996-654539 A 19960529
AIT TWA patent application
PRAIT USA patent application
ICM (7) H01L021-60

1996 priority

AB Microelectronic packages are formed wherein **solder** bumps on one or more substrates are expanded, to thereby extend and contact the second substrate and form a **solder** connection. The **solder** bumps are preferably expanded by reflowing additional **solder** into the plurality of **solder** bumps. The additional **solder** may be reflowed from an **elongated**, narrow **solder**-containing region adjacent the **solder** bump, into the **solder** bump. After reflow, the **solder** bump which extends across a pair of adjacent substrates forms an arched **solder column** or partial ring of **solder** between the two substrates.

L121 ANSWER 3 OF 9 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-291248 [33] WPIX
CR 1992-132352 [16]; 1994-293619 [36]; 1997-525801 [48]; 1997-558042 [51]; 1999-069315 [06]; 1999-080544 [07]; 1999-560234 [47]; 2001-201283 [20]; 2002-237703 [29]
DNN N2002-227398
TI Semiconductor chip assembly for electronic device, has resilient element which enables movement of terminals of sheet-like dielectric interposer towards semiconductor chip.
DC U11
IN DISTEFANO, T H; KHANDROS, I Y
PA (DIST-I) DISTEFANO T H; (KHAN-I) KHANDROS I Y; (TESS-N) TESSERA INC
CYC 1
PI US 2002011663 A1 20020131 (200233)* 39p H01L023-48
US 6433419 B1 20020813 (200261) H01L023-053
PRAI US 1991-765928 19910924; US 1990-586758 19900924; US 1991-673020 19910321; WO 1991-US6920 19910924; US 1993-30194 19930428; US 1994-319966 19941007; **US 1997-861280 19970521**; **US 1997-984615 19971203**; US 2000-488268 20000120
AB US2002011663 A UPAB: 20020924
NOVELTY - A **flexible** sheet-like dielectric interposer (42) is positioned between a semiconductor chip (28) and a substrate (20). Several terminals (48) of the interposer are arranged such that they overlie the front surface of the chip. A resilient element such as a **compliant** layer is provided for enabling movement of the terminals (48) towards the semiconductor chip.

USE - For electronic device.

ADVANTAGE - Enables movement of the interposer terminals with respect to the chip, so as to compensate for **thermal expansion**

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor chip assembly.
Substrate 20
Semiconductor chip 28
Flexible sheet-like dielectric interposer 42
Terminals 48
Dwg.2/30
FS EPI
FA AB; GI
MC EPI: U11-D01C6; U11-D03A2

applicant
5/21/97
priority

L124 ANSWER 9 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1999-547022 [46] WPIX
DNN N1999-406182 DNC C1999-159901
TI Wafer scale assembly for chip size **package** and integrated circuits - involves binding wafer with several circuits equipped with metal contact pad and polymer film having patterned **solder** ball of uniform height.
DC L03 U11
IN AMADOR, G; HEINEN, K G; HOTCHKISS, G G; HOTCHKISS, G B
PA (TEXI) TEXAS INSTR INC
CYC 27
PI JP 11238832 A 19990831 (199946)* 14p H01L023-12
EP 955676 A2 19991110 (199952) EN H01L023-31
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
US 6432744 B1 20020813 (200255) H01L021-44
ADT JP 11238832 A JP 1998-330912 19981120; EP 955676 A2 EP 1998-203877 19981120; US 6432744 B1 Provisional US 1997-66268P 19971120, US 1998-183980 19981031
PRAI **US 1997-66268P 19971120**; US 1998-183980 19981031
IC ICM H01L021-44; H01L023-12; H01L023-31
ICS H01L021-48; H01L021-50; H01L021-60; H01L021-8222; H01L023-498
AB JP 11238832 A UPAB: 19991110
NOVELTY - A semiconductor wafer equipped with several circuits has a metal contact pad. A polymer film (10) with wafer scale patterned, has **solder** ball (12) with uniform height irrespective of shape and volume. The film is made to contact with the wafer and radiant energy of infrared rays are irradiated from back side of wafer. DETAILED DESCRIPTION - The reflow of **solder** ball is performed on contact pad and **elongation** by the heat of polymer film is compensated mechanically. The uniformity in height of **solder** ball in liquid state is controlled by mechanical stopper etc. After cooling, it solidifies and **solder** ball removes polymer film. The process is repeated.

USE - For chip size packages used in pager, hard disk drive, lap-top computer, in appliance for medical science.

ADVANTAGE - Offers quick heating of wafer and uniform reflow procedure. Offers uniform mechanical positioning control and **heat cycle**. DESCRIPTION OF DRAWING(S) - The figure shows partial sectional view of plastic film. (10) Polymer film; (12) **Solder** ball.

Dwg.1/17
FS CPI EPI
FA AB; GI

L124 ANSWER 12 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1999-071860 [07] WPIX
DNN N1999-052538 DNC C1999-021536
TI Low temperature **soldering** using high melting temperature **solder** - by providing exothermically reactive component at **soldering** location.
DC L03 M23 M26 P55 V04 X24
IN ALBRECHT, H; BEREK, H; DOERR, M; HAERTEL, W; HANNEMANN, M; PACHSCHWOELL, H; SCHEEL, W; WITTKE, K
PA (BGME-N) BG METALLWERK GOSLAR GMBH & CO KG; (FRAU) FRAUNHOFER GES FOERDERUNG ANGEWANDTEN; (MATE-N) ZENT MATERIAL & UMWELTTECHNIK GMBH; (META-N) METALLWERK GOSLAR GMBH & CO KG
CYC 20
PI DE 19728014 A1 19990107 (199907)* 4p B23K001-00
WO 9901250 A1 19990114 (199909) DE B23K035-34
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 939684 A1 19990908 (199941) DE B23K035-34
R: BE DE DK ES FI FR GB IT LU NL SE
ADT DE 19728014 A1 DE 1997-19728014 19970701; WO 9901250 A1 WO 1998-EP3974 19980629; EP 939684 A1 EP 1998-939558 19980629, WO 1998-EP3974 19980629
FDT EP 939684 A1 Based on WO 9901250
PRAI **DE 1997-19728014 19970701**
IC ICM B23K001-00; B23K035-34
ICS B23K035-26
AB DE 19728014 A UPAB: 19990217
In a metal **soldering** process, the **soldering** location is supplied with a reaction component which, on heating to an activation temperature (especially about 221 deg. C), reacts exothermically with another component for local heating to the **soldering** temperature. Preferably, the **solder** is a tin **solder** (e.g. SnCu or **SnCuPb**) and the reaction component may be (a) Pd and/or SnAg 3.5 (as initiating eutectic) mixed with or coated on the **solder**; (b) an organic or inorganic metal salt, e.g. cobalt (II) acetylacetonate; or (c) a metal-free reagent, e.g. n-nonane, which may also act as a flux.

Also claimed is a **solder** used in the above process.

USE - E.g. for **soldering** temperature sensitive electronic components onto circuit boards using **solder** pastes.

ADVANTAGE - The process employs a relatively low heating temperature for reaction initiation to produce the melting temperature locally within the **solder**, thus permitting the use of **solders** with increased melting temperatures without the need for external supply of the heat required for **solder** melting.

Dwg.0/0
FS CPI EPI GMPI

L123 ANSWER 7 OF 10 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2001-380309 [40] WPIX
CR 2000-052136 [04]
DNN N2001-278774
TI Microelectronic element connector has pedestal that supports lead and deflects in horizontal direction.
DC U11 V04
IN FJELSTAD, J
PA (TESS-N) **TESSERA INC**
CYC 1
PI US 6229100 B1 20010508 (200140)* 17p H01R012-04
ADT US 6229100 B1 Provisional US 1996-31948P 19961127, Div ex US 1997-999758 19971126, US 1999-234650 19990121
FDT US 6229100 B1 Div ex US 5983492
PRAI US 1996-31948P 19961127; **US 1997-999758 19971126**; US 1999-234650 19990121
IC ICM H01R012-04
ICS H05K001-11
AB US 6229100 B UPAB: 20010719
NOVELTY - Electrically conductive **elongated** leads (300) overlying the substrate, have contact portions that contact the element terminal and underly a complaint layer. A pedestal (700) is partially isolated from the remaining portion of the complaint layer by gaps (701) in the complaint layer. The pedestal deflects horizontally, compensating for relative movement between the connector and the microelectronic element.

USE - For connecting microelectronic element having array of element terminals, also as socket for testing and burn-in of microelectronic elements.

ADVANTAGE - Pedestal improves the reliability of the **solder** joint interconnection by permitting movement of the **contact** to compensate for the coefficient of **thermal expansion** mismatch between the microelectronic element and the substrate.

DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view and partial diagrammatic view of the microelectronic connector.
Lead 300
Pedestal 700
Gap 701
1H, 3B/11

1996 priority

L124 ANSWER 8 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-040117 [05] WPIX
DNN N2002-029646 DNC C2002-011386
TI Ball grid array **interconnection** structure, comprises spheres joined to module by electrically conductive adhesive comprising thermoplastic or thermosetting resin matrix, no-clean **solder** flux and conductive particles.
DC A85 L03 U11
IN CALL, A J; DELAURENTIS, S A; FAROOQ, S; KANG, S K; PURUSHOTHAMAN, S; STALTER, K A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6297559 B1 20011002 (200205)* 10p H01L023-48
ADT US 6297559 B1 Provisional US 1997-52175P 19970710, US 1998-107998 19980630
PRAI **US 1997-52175P 19970710**; US 1998-107998 19980630
IC ICM H01L023-48
AB US 6297559 B UPAB: 20020123
NOVELTY - Ball grid array structure has electrically conductive spheres joined to a chip carrier module by electrically conductive adhesive (ECA) and printed wiring board by **solder** paste respectively. ECA contains thermoplastic/thermosetting polymer resin matrix, no-clean **solder** flux and electrically conductive particles (EP) having electrically conductive fusible coating. Some EP are fused through the coating.

DETAILED DESCRIPTION - Ball gid array structure comprises an array of electrically conductive spheres (34), disposed on an electronic chip carrier module (31). The spheres are electrically and mechanically joined to terminal pads on the module by an electrically conductive adhesive (33). The spheres are electrically and mechanically joined to printed circuit board (36) by **solder** paste (35). The conductive adhesive comprises thermoplastic or thermosetting polymer resin matrix, no-clean **solder** flux and several electrically conductive particles. The electrically conductive particles are coated by electrically conductive and fusible coating. At least some of conductive particles are fused with each other through electrically conductive fusible coating.

USE - For interconnecting micro-electronic packages and printed circuit boards.

ADVANTAGE - The structure such as ball grid array package (BGA) has longer **fatigue** life. The structure provides stronger and **compliant** interconnections of ball grid array package to ceramic or plastic substrates. BGA structure is stable and does not cause an excessive inter diffusion between **solder** ball and adjoining **solder** paste.

DESCRIPTION OF DRAWING(S) - The figures show the schematic cross-sectional representation of new **solder** ball connection scheme in ceramic ball grid array package.

Module 31
Electrically conductive adhesive 33
Spheres 34
Solder paste 35
Printed circuit board 36

Dwg.3, 5/5
TECH US 6297559 B1 UPTX: 20020123
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The electrically conductive particle is formed from material(s) chosen from **copper**, silver, gold, aluminum, palladium, and platinum. The conductive spheres are made of material(s) chosen from **lead**, **tin**, indium, bismuth, antimony and/or zinc. The electrical coating is chosen from tin, zinc, indium, lead, bismuth and/or antimony. Preferred Properties: The conductive particles have diameter of 1-50 mum. The thickness of fusible coating layer is 0.1-2 mum. Preferred Process: The spheres are attached using conductive adhesive by applying heat and pressure for preset time. The polymeric material provides adhesive joining of terminal pads.

TECHNOLOGY FOCUS - POLYMERS - Preferred Compounds: The polymeric material is polyimide, siloxane, polyimide-siloxane, phenoxypolymer, styrene allyl

alcohol polymers, epoxies or bio-based polymeric resin chosen from lignin, cellulose, wood oil and crop oil.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The structure is electronic device, computing device or ball grid array package. The chip carrier module is metallized ceramic, multi-layered cofired ceramic, organic film optionally provided with rigid frame or printed wiring board portion.
Preferred Structure: The spheres are electrically and mechanically joined to terminal pads of printed circuit board by another electrically conductive adhesive. The electronic chip carrier module is electrically connected to integrated circuit device by an array of conductive bumps made of an electrically conductive adhesive.

ABEX US 6297559 B1 UPTX: 20020123
WIDER DISCLOSURE - Interconnection scheme of ball grid array package to ceramic and organic substrate by electrically conductive material, and method for forming an electrically conductive joint between a solder ball and contact pad, are disclosed.

FS CPI EPI

FA AB; GI

MC CPI: A08-M09A; A09-A03; A11-C01C; A12-E07A; A12-E07C; **L04-C17A**
EPI: U11-D03A

PLE UPA 20020123

L101 ANSWER 2 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:113140 HCAPLUS
DN 132:155344
TI Soldering column with the Pb-In-Sn alloy zone for joining of electronic components by the controlled-collapse chip connection with increased resistance to fatigue
IN Digiacomo, Giulio
PA International Business Machines Corporation, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT **Patent**
LA English
IC ICM H01L023-48
ICS **H01L023-52**; H01L029-40
NCL 257779000
CC 56-9 (Nonferrous Metals and Alloys)
Section cross-reference(s): 76
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6025649	A	20000215	US 1997-898443	19970722
	TW 411744	B	20001111	TW 1998-87103419	19980309 <--
	US 6196443	B1	20010306	US 1998-118117	19980716 <--
	US 6329721	B1	20011211	US 2000-570884	20000515 <--
PRAI	US 1997-898443	A	19970722 <--		
	US 1998-118117	A3	19980716 <--		

AB The solder column structure suitable for joining of electronic components comprises: (a) Pb-(1-5%) Sn alloy solder column nominally 9-15 mils high attached at one end to a substrate; and (b) In layer 0.5-2 mils thick at the other end. During reflow soldering the In layer is melted with a part of the solder column, forming the Pb-Sn-In ternary alloy joint having increased fatigue resistance. The ternary Pb alloy has nominal compn. of 40% In and 1.8% Sn.
IT **12610-69-4 91145-76-5**
RL: TEM (Technical or engineered material use); USES (Uses)
(**solder**; **soldering** column with Pb-Sn alloy and In layer for joining of electronic components by controlled-collapse chip connection)
RN 12610-69-4 HCAPLUS
CN Lead alloy, base, Pb 97,Sn 3 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	97	7439-92-1
Sn	3	7440-31-5

RN 91145-76-5 HCAPLUS
CN Lead alloy, base, Pb 95-99,Sn 1-5 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	95 - 99	7439-92-1
Sn	1 - 5	7440-31-5

L123 ANSWER 2 OF 10 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 147866455 INPADOC ED 20010410 EW 200114 UP 20030317 UW 200311
TI SEMICONDUCTOR CHIP ASSEMBLY
IN MITCHELL CRAIG; WARNER MIKE; BEHLEN JIM
INS MITCHELL CRAIG; WARNER MIKE; BEHLEN JIM
INA US; US; US
PA **TESSERA, INC**
PAS TESSERA INC
PAA US
DT **Patent**
PIT USBA PATENT (NO PREVIOUS PRE-GRANT PUBLICATION)
PI US 6169328 BA 20010102
AI US 1999-246056 A 19990208
PRAI **US 1999-246056 A 19990208**
US 1997-842313 A2 19970424
US 1994-365699 A3 19941229
US 1994-309433 B2 19940920
AIT USA patent application
PRAIT USA patent application
USA2 appl. number is cited as basic appl. number for a continuation in part
USA3 appl. number is cited as basic appl. number from which a division was made
USB2 abandoned appl. number is cited as basic appl. number for a continuation in part
RLI US 5659952 now patented
ICM (7) H01L023-48
ICS **(7) H01L023-52**; (7) H01L029-40
EPC H01L21/56F; H01L21/60C4; H01L23/48F; H01L23/498C; H01L23/498E
NCL 257778; X257786; X257787; X257789; X257675; X257719
AB A semiconductor chip package structure for providing a reliable interface between a semiconductor chip and a PWB to accommodate for the thermal coefficient of **expansion** mismatch therebetween. The interface between a chip and a PWB is comprised of a package substrate having a plurality of **compliant** pads defining channels therebetween. The package substrate is typically comprised of a **flexible** dielectric sheet that has leads and terminals on at least one surface thereof. The pads have a first coefficient of **thermal expansion** ("**CTE**") and are comprised of a material having a fairly low modulus of elasticity. An encapsulant having a second **CTE** lower than the **CTE** of the **compliant** pads is disposed within the channels to form a uniform encapsulation layer. The pads are in rough alignment with the conductive terminals on the package substrate thereby allowing independent movement of the terminals during thermal cycling of the chip. The encapsulant encases the conductive leads electrically connecting the terminals to chip contacts on a face surface of the chip. The lower **CTE** of the encapsulant controls the **flexing** of the conductive leads so that the leads do not prematurely **fatigue** and become unreliable while the lower modulus **compliant** pads relieve the stress on the **solder** balls induced by the **CTE** mismatch of the chip and the PWB.

applicant

1994 priority

L123 ANSWER 8 OF 10 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2001-181459 [18] WPIX
CR 1996-097761 [10]; 1996-188719 [19]; 1997-203137 [18]; 1997-203234 [18]; 1998-007997 [01]; 1998-086369 [08]; 1998-378040 [32]; 1998-543009 [46]; 2002-664788 [71]; 2003-138880 [13]; 2003-298282 [29]; 2003-531038 [50]
DNN N2001-129391 DNC C2001-054064
TI Semiconductor chip package includes encapsulant and **compliant** pads of **different** coefficient of **thermal expansion** that forms composite layer between chip unit and substrate.
DC A85 L03 U11
IN BEHLEN, J; MITCHELL, C; WARNER, M
PA (TESS-N) **TESSERA INC**
CYC 1
PI US 6169328 B1 20010102 (200118)* 19p H01L023-48
ADT US 6169328 B1 CIP of US 1994-309433 19940920, Div ex US 1994-365699 19941229, CIP of US 1997-842313 19970424, US 1999-246056 19990208
FDT US 6169328 B1 Div ex US 5659952
PRAI US 1999-246056 19990208; US 1994-309433 19940920; US 1994-365699 19941229; **US 1997-842313 19970424**
IC ICM H01L023-48
ICS **H01L023-52**; H01L029-40
AB US 6169328 B UPAB: 20030805
NOVELTY - The **compliant** pads (110) are juxtaposed with surface of substrate and attached with chip unit (120). The chip contacts are connected to terminals on substrate surface via leads. The encapsulant surrounds pads so that encapsulant and pads form composite layer between chip unit and substrate. Coefficient of **thermal expansion** (**CTE**) of the encapsulant and pads are 50-400 ppm/ deg. C and 15-300 ppm/ deg. C respectively.

DETAILED DESCRIPTION - The inner and outer terminals are exposed at one of the substrate surface. The inner terminals are located within periphery of the chip and outer terminals located beyond the periphery of chip and above the **compliant** pads. The **compliant** pads have modulus of elasticity between 1-300 MPa and encapsulant has modulus of elasticity between 10 MPa-8 GPa. The **compliant** pads and chip units are made up of materials selected from the group containing silicones, epoxies, urethanes, gels, foams and combinations, blends and composite of such materials. Planar sheet like heat spreader is attached to back surface of chip and to encapsulant.

USE - Semiconductor chip package with suitable interface between semiconductor chip and PWB, in fan-in or fan-out package structure.

ADVANTAGE - The lower **CTE** of encapsulant controls **flexing** of leads so that leads do not prematurely **fatigue** and become unreliable while the lower modulus **compliant** pads relieve the stress on **solder** balls induced by **CTE** mismatch of chip and PWB. The pads are in rough alignment with the conductive terminals on the package substrate, thereby allowing independent movement of terminals during thermal cycling of chip. The **compliant** pad material is silicone fitted with fumed and/or fused silica to obtain the desired modulus.

DESCRIPTION OF DRAWING(S) - The figure shows the side view of **compliant** semiconductor chip interface.

Compliant pads 110
Chip unit 120
Dwg.1/10
FS CPI EPI
FA AB; GI
MC CPI: A12-E07C; L04-C11; L04-C20

L123 ANSWER 3 OF 10 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 138675159 INPADOC ED 20001114 EW 200045 UP 20030630 UW 200326
TI SEMICONDUCTOR CHIP PACKAGE WITH CENTER CONTACTS
IN KHANDROS, IGOR Y.; DISTEFANO, THOMAS H.
INS KHANDROS IGOR Y; DISTEFANO THOMAS H
INA US; US
PA **TESSERA, INC.**
PAS TESSERA INC
PAA US
DT **Patent**
PIT USA UNITED STATES PATENT
PI US 6133627 A 20001017
AI US 1997-984615 A 19971203
PRAI **US 1997-984615 A 19971203**
US 1997-861280 A3 19970521
US 1994-319966 A1 19941007
US 1991-765928 A1 19910924
US 1991-673020 A2 19910321
US 1990-586758 A2 19900924

assignee

AB A semiconductor chip having contacts on the central region of its top surface is provided with a dielectric element overlying the central portion of the top surface. The dielectric element has a first surface facing toward the chip and a second surface facing away from the chip, a hole encompassing the central contacts and an edge bounding the hole. Central contact leads extend from the central contacts on the chip to central terminals on the dielectric element. The terminals on the dielectric element may be connected to a substrate using techniques commonly employed in surface mounting of electrical devices, such as **solder** bonding. The leads, and preferably the dielectric element, are **flexible** so that the terminals are moveable with respect to the contacts on the chip, to compensate for **differential thermal expansion** of the chip and substrate. The dielectric element may be provided with a **compliant** layer disposed between the terminals and the chip. The entire assembly is compact.

L123 ANSWER 9 OF 10 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2000-052136 [04] WPIX
CR 2001-380309 [33]
DNN N2000-040661
TI Connector manufacturing method for semiconductor integrated chips and other electronic components mounted on printed circuit boards used in microelectronic device.
DC T01 V04
IN FJELSTAD, J
PA (TESS-N) **TESSERA INC**
CYC 1
PI US 5983492 A 19991116 (200004)* 17p H01R009-00
ADT US 5983492 A Provisional US 1996-31948P 19961127, US 1997-999758 19971126
PRAI US 1996-31948P 19961127; **US 1997-999758 19971126**
IC ICM H01R009-00
AB US 5983492 A UPAB: 20010719
NOVELTY - A photoresist layer is formed over **elongated** metallic leads (300) on top surface of substrate for defining open areas over the respective ends of leads. Compliant pedestals (750) are formed by filling the open areas in the photoresist layer with compliant material. The substrate and photoresist layer are removed so that the pedestals support the ends of the leads.

USE - For manufacturing connector for semiconductor integrated chips and other microelectronic components in microelectronic devices especially for designs associated with PCMCIA cards for laptop computer.

ADVANTAGE - Reliability of **solder** joint interconnection is improved by permitting movement of **contact** to compensate for coefficient of **thermal expansion** mismatch between the microelectronic device and substrate. The compliant pedestals function absorbs lateral forces in response to thermally generated forces similar to that involved in absorption of forces generated during positioning of component in the socket. Thereby protects mechanical and electrical connections between the socket and microelectronic device. By partially or completely separating the pedestal from other portions of compliant layer, deflection within the pedestal is localized and does not affect those portions of compliant layer from which the pedestal is separated. Facilitates to manufacture large number and wide variety of sockets simultaneously on PCB.

DESCRIPTION OF DRAWING(S) - The figure shows the diagrammatic perspective view of connector.
Leads 300
Compliant pedals 750
Dwg.4/11
FS EPI
FA AB; GI
MC EPI: T01-L09; V04-M01; V04-M05; V04-M30E; V04-P

1996 priority

L123 ANSWER 4 OF 10 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 48020583 INPADOC EW 199838 UP 20030505 UW 200317
TI MICROELECTRONIC MOUNTING WITH MULTIPLE LEAD DEFORMATION AND BONDING
IN DISTEFANO, THOMAS H.; SMITH, JOHN W.
INS DISTEFANO THOMAS H; SMITH JOHN W
INA US; US
PA **TESSERA, INC.**
PAS TESSERA INC
PAA US
DT **Patent**
PIT USA UNITED STATES PATENT
PI US 5801441 A 19980901
AI US 1995-440665 A 19950515
PRAI US 1995-440665 A 19950515
US 1994-271768 A3 19940707
AIT USA patent application
PRAIT USA patent application
USA3 appl. number is cited as basic appl. number from which a division was made
RLI US 5518964 now patented
ICM (6) H01L023-48
ICS **(6) H01L023-52**; (6) H01R009-09; (6) H01R004-58
EPC H01L21/48C3L; H01L23/22; H01L23/48F; H01L23/498C; H01L23/498C4; H01L23/498E; H01L23/498J; H01L23/64C; H05K3/40D6
NCL 257696; X257688; X257689; X257692; X439 66; X439 91
AB A microelectronic connection component includes a dielectric sheet having an area array of **elongated**, strip-like leads. Each lead has a terminal end fastened to the sheet and a tip end detachable from the sheet. Each lead extends horizontally parallel to the sheet, from its terminal end to its tip end. The tip ends are attached to a second element, such as another dielectric sheet or a semiconductor wafer. The first and second elements are then moved relative to one another to advance the tip end of each lead vertically away from the dielectric sheet and deform the leads into a bent, vertically extensive configuration. The preferred structures provide semiconductor chip assemblies with a planar area array of contacts on the chip, an array of terminals on the sheet positioned so that each terminal is substantially over the corresponding contact, and an array of metal S-shaped ribbons connected between the terminals and contacts. A **compliant** dielectric material may be provided between the sheet and chip, substantially surrounding the S-shaped ribbons.

L124 ANSWER 16 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-201082 [20] WPIX
DNN N1996-168699
TI **Solder** bearing lead manufacturing method for PCB components e.g. chip carriers, IC's - using continuous strip of lead blanks with reduced width section formed on each blank which retains rosin cored **solder** bead.
DC U11 V04
IN POLLOCK, L J; SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES
CYC 65
PI WO 9610279 A1 19960404 (199620)* 34p H01R009-09
AU 9539549 A 19960419 (199630) H01R009-09
US 5601459 A 19970211 (199712) 9p H01R004-02
EP 783775 A1 19970716 (199733) EN H01R009-09
R: DE FR GB
US 5688150 A 19971118 (199801) 13p H01R004-02
EP 783775 B1 20000503 (200026) EN H01R012-04
R: DE FR GB
DE 69516704 E 20000608 (200034) H01R012-04
PRAI US 1995-512508 19950808; US 1994-315204 19940929
REP US 3864014; US 3915546; US 4302067; US 4367910; US 4605278; US 4900279; US 5030144
IC ICM H01R004-02; H01R009-09; H01R012-04
ICS H01R012-32
AB WO 9610279 A UPAB: 19960520
The **solder** bearing leads are manufactured from a continuous strip of conductive material which is passed through a stamping machine to produce a series of lead blanks joined at one end to a carrier strip. At the position where a **solder mass** is to held each lead blank has a reduced width section with shoulders at each end which form stops to prevent the **solder mass** from moving along the lead. During fabrication the lead is bent slightly at the position of the reduced width section and a rosin cored **solder** wire is laid across several leads at their reduced width locations. The **solder** wire is then severed on each side of the reduced width section to form a bead of **solder** surrounding the reduced section.
ADVANTAGE-Allows miniaturisation by permitting closer spacing of contact pads on PCB substrates
Dwg.28/34
ABEQ US 5601459 A UPAB: 19970320
A connector arrangement for a substrate having a row of conductive pads, comprising:
a carrier strip of electrically conductive material of substantially uniform thickness,
a plurality of **elongated** conductive leads, each integrally connected to said carrier strip at one end of the lead, said leads being parallel and spaced corresponding to said pads,
each lead comprising:
a generally flat body portion of substantially uniform width and thickness, with an upper surface and a lower surface,
a longitudinally extending **solder**-bearing portion at a predetermined position along said lead adjoining said flat body portion and having a cross-section with undercuts at the edges of said **solder**-bearing portion, an interior portion of said cross-section having a tip extending at least to the same extent as the lower surface of said adjoining flat body portion,
a shoulder between said **solder**-bearing portion and said flat body portion at an end of said **solder**-bearing portion, and
a **solder mass** mechanically formed about said **solder**-bearing portion, and extending around said undercuts and substantially to said tip, said **solder mass** formed at a temperature below the melting point of said **solder mass**,
whereby said **solder mass** is prevented from longitudinal movement by said shoulder and from transverse movement by said undercuts, and said lead may be **soldered** to a corresponding

pad by placing said tip in contact with said pad and reflowing said **solder mass**.
Dwg.1,3/24
ABEQ US 5688150 A UPAB: 19980107
The **solder** bearing leads are manufactured from a continuous strip of conductive material which is passed through a stamping machine to produce a series of lead blanks joined at one end to a carrier strip. At the position where a **solder mass** is to held each lead blank has a reduced width section with shoulders at each end which form stops to prevent the **solder mass** from moving along the lead. During fabrication the lead is bent slightly at the position of the reduced width section and a rosin cored **solder** wire is laid across several leads at their reduced width locations. The **solder** wire is then severed on each side of the reduced width section to form a bead of **solder** surrounding the reduced section.
ADVANTAGE-Allows miniaturisation by permitting closer spacing of contact pads on PCB substrates
1,2,23/34
FS EPI

L121 ANSWER 2 OF 9 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 37344807 INPADOC UP 20030630 UW 200326
TI SEMICONDUCTOR CHIP ASSEMBLIES, METHODS OF MAKING SAME AND COMPONENTS FOR SAME
IN KHANDROS, IGOR Y.; DISTEFANO, THOMAS H.
INS KHANDROS IGOR Y; DISTEFANO THOMAS H
INA US; US
PA TESSERA, INC.
PAS TESSERA INC
PAA US
DT **Patent**
PIT USA UNITED STATES PATENT
PI US 5679977 A 19971021
AI US 1993-30194 A 19930428
PRAI US 1993-30194 A 19930428
US 1990-586758 A2 19900924
US 1991-673020 A2 19910321
US 1991-765928 A1 19910924
AB Semiconductor chip assemblies incorporating **flexible**, sheet-like elements having terminals thereon overlying the front or rear face of the chip to provide a compact unit. The terminals on the sheet-like element are movable with respect to the chip, so as to compensate for **thermal expansion**. A resilient element such as a **compliant** layer interposed between the chip and terminals permits independent movement of the individual terminals toward the chip driving engagement with a test probe assembly so as to permit reliable engagement despite tolerances.

L121 ANSWER 5 OF 9 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1997-525801 [48] WPIX
CR 1992-132352 [16]; 1994-293619 [36]; 1997-558042 [51]; 1999-069315 [06]; 1999-080544 [07]; 1999-560234 [44]; 2001-201283 [63]; 2002-237703 [69]; 2002-291248 [21]
DNN N1997-438212
TI Semiconductor chip assembly for electronic packaging - uses **flexible** sheetlike element, between substrate and chip, upon which terminals link with contacts on overlaid chip surface by **flexible** leads.
AW FIRST-LEVEL ASSEMBLY.
DC U11
IN DISTEFANO, T H; KHANDROS, I Y
PA (TESS-N) TESSERA INC
CYC 1
PI US 5679977 A 19971021 (199748)* 39p H01L023-48
ADT US 5679977 A CIP of US 1990-586758 19900924, CIP of US 1991-673020 19910321, Cont of US 1991-765928 19910924, Cont of WO 1991-US6920 19910924, US 1993-30194 19930428
FDT US 5679977 A CIP of US 5148265, CIP of US 5148266, Cont of US 5347159
PRAI US 1991-765928 19910924; US 1990-586758 19900924; US 1991-673020 19910321; WO 1991-US6920 19910924; US 1993-30194 19930428
IC ICM H01L023-48
ICS **H01L023-52**
AB US 5679977 A UPAB: 20020524
The assembly has a chip (28) with several surfaces (36,38), contacts (40) present on at least one surface. Between the substrate (20) and chip is placed a **flexible** sheetlike element (42) that includes an elastomeric **compliant** layer. Upon one surface (46) of the element are terminals (48). These link to the contacts via **flexible** leads (50). The upper surface (44) of the element faces the chip surface (38) with contacts on. Apertures (54) in the element align with the contacts.

The leads have a contact end (56) bonded to the contact with the other end joining with the terminal. The leads and element, both being **flexible** in nature, are able to undergo deformation e.g. buckling, wrinkling, compression, tension. This allows each terminal to be moveable with respect to its corresponding chip contact in directions parallel to chip surface.

ADVANTAGE - Compensates for **thermal expansion** and facilitates temporary contact of terminals by test equipment for test and burn-in of assembly.

Dwg.2,3/30
FS EPI
FA AB; GI
MC EPI: U11-D03A; **U11-D03B**; U11-E02A2

Applicant

1993 priority

L124 ANSWER 13 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1997-077668 [07] WPIX
DNN N1997-064425
TI **Flexible** leads for tape ball grid array circuit, such as quad flat pack IC - includes via holes and circuitry on polymeric sheet, terminating at cantilever end spanning via hole to which **solder** ball is attached.
DC U11
IN SCHUELLER, R D; WINDSCHITL, D J
PA (MINN) MINNESOTA MINING & MFG CO
CYC 25
PI WO 9700537 A1 19970103 (199707)* EN 12p H01L023-498
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA CN FI JP KR NO SG
US 5602422 A 19970211 (199712) 6p H01L023-48
EP 834195 A1 19980408 (199818) EN
R: CH DE FI FR GB IT LI NL SE
NO 9705843 A 19980216 (199818)
JP 11507769 W 19990706 (199937) 13p H01L023-12
KR 99022864 A 19990325 (200024) H01L023-498
CN 1186570 A 19980701 (200266) H01L023-498
ADT WO 9700537 A1 WO 1996-US6373 19960503; US 5602422 A US 1995-491229 19950616; EP 834195 A1 EP 1996-915537 19960503, WO 1996-US6373 19960503; NO 9705843 A WO 1996-US6373 19960503, NO 1997-5843 19971211; JP 11507769 W WO 1996-US6373 19960503, JP 1997-503051 19960503; KR 99022864 A WO 1996-US6373 19960503, KR 1997-709333 19971212; CN 1186570 A CN 1996-194355 19960503
FDT EP 834195 A1 Based on WO 9700537; JP 11507769 W Based on WO 9700537; KR 99022864 A Based on WO 9700537
PRAI US 1995-491229 19950616
REP 1.Jnl.Ref; DE 4417670; EP 349000; EP 532898; JP 62030342; US 5203075; US 5359222; US 5420460
IC ICM H01L023-12; H01L023-48; H01L023-498
ICS H01L021-60; **H01L023-52**; H01L029-40
AB WO 9700537 A UPAB: 19970212
A **flexible** circuit board is constructed to include a cantilever beam which spans a via hole at the end of the circuitry terminating at a lead. A **solder** ball is attached to the beam which is bend down. This gives the ball mobility relative to the circuit reducing levels of stress.
The circuit structure comprises a **flexible** polymeric sheet. The via hole may extend along the lead or the sheet may be cut adjacent the lead to increase the effective length of the cantilever end to increase **flexibility**.
ADVANTAGE - Resistant to **fatigue** stresses due to **differences** in coeffts. of **thermal expansion**.
Dwg.1/6
ABEQ US 5602422 A UPAB: 19970320
A **flexible** circuit for attachment to a printed circuit board, said **flexible** circuit comprising:
a base comprising a **flexible** polymeric sheet, said base having two major surfaces;
a via hole through said base;
a conductive trace disposed on a first major surface of said base and defining electrical circuitry terminating at a cantilever end spanning a portion of said via hole, said cantilever end being angularly displaced from said conductive trace to extend into said via hole;
an **elongate** slit **terminating** at one end thereof at said via hole to permit greater movement of said cantilever end relative to the plane of said **flexible** polymeric sheet; and
a **solder** ball attached to said cantilever end from a second major surface of said base such that a subsequent attachment of a printed circuit board to said **flexible** circuit from said second major surface will accommodate physical displacement of said **flexible** circuit and said printed circuit board.
Dwg.4/6
FS EPI

L124 ANSWER 15 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-278048 [28] WPIX
CR 1995-200548 [26]; 1996-260007 [26]; 1996-260008 [26]; 1996-260071 [26];
TI Electrical contact structure fabrication for **connecting** device to PCB - by configuring **flexible elongate** member and overcoating with electroconductive material.
DC A85 L03 S01 U11 V04
IN ELDRIDGE, B N; GRUBE, G W; KHANDROS, I Y; MATHIEU, G; MATHIEU, G L
PA (FORM-N) FORMFACTOR INC
CYC 65
PI WO 9617378 A1 19960606 (199628)* EN 423p H01L021-60
AU 9642839 A 19960619 (199640)
EP 792517 A1 19970903 (199740) EN
R: CH DE FR GB IT LI
KR 97707575 A 19971201 (199847) H01L021-60
JP 11514493 W 19991207 (200008) 398p H01L023-32
EP 1198001 A2 20020417 (200233) EN H01L021-66
PRAI US 1995-554902 19951109; US 1994-340144 19941115; WO 1994-US13373 19941116; US 1995-452255 19950526; US 1995-457479 19950601; US 1995-526246 19950921; US 1995-533584 19951018
AB WO 9617378 A UPAB: 20030619
An electrical contact structure is fabricated by configuring a **flexible elongate** member to have a springable shape, and applying an overcoat.

Also claimed are : (a) a method of electrically interconnecting the electronic components by bonding a flexible wire to a contact area on a 1st component, continuing the wire to a springable shape, serving to produce a distal end, overwater the wire and contact area with electroconductive resilient material, and contacting the distal end with the 2nd component; (b) fabricating an interpreter by forming resilient contact structures through holes in a substrate, on a removing a sacrificial substrate; (c) mounting multiple contact structures to an electronic component, (d) a testing and hum-in method involving electrically connecting the tips of the resilient contacts to the contact areas of a test broad, then mounting the device to a system board; (e) temporary connection of the device prior to permanent connection; (f) another method of connecting the components; (g) an electronic assembly composed of semiconductor dies mounted edge-to-edge and connected to a PCB by the resilient contact structure; (h) creating a superstructure on a falsework; (i) tailoring the thickness of a plating by creating a temp. gradient during plating; (j) making two or more free standing resilient contact structures; (k) forming a protruberant conductive contact to a component; (l) mfg. electrical contacts on a surface of an electronic components; (m) connecting 1st and 2nd components via a 3rd component, and via resilient contact structures; (n) an interposer comprising a dielectric substrate with conductive areas and resilient contact structures; (o) an interposer with holes in the substrate, each hole contg. a contact structure; (p) a semiconductor package; (q) a semiconductor device with free-standing heat dissipating structures on the back at the die; (r) a method assembling an electronic assembly; (s) a method of mounting a free-standing contact structure to an electronic component; (t) forming a ball at an end of a wirebond wire, and (u) making engineering changes in an interposer.

ADVANTAGE - Plastic and elastic deformation of the contact structure can be tailored to the intended application. The rigidity of the wire bond is improved, can behave as a spring and is firmly anchored to the terminal. Direct mounting to dies before or after sepn. from the wafer is possible. The structures allow temporary connection for testing.

Dwg.5/54
FS CPI EPI
FA AB; GI
MC CPI: A05-A01E2; A11-B05; A12-E01; L03-H04E6; **L04-C17A**; L04-C18; L04-C25; L04-F02
EPI: S01-H03; U11-E01A; U11-F01C1; U11-F01G; V04-Q02A; V04-R04
PLE UPA 20030619

L124 ANSWER 14 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-437844 [44] WPIX
DNN N1996-368991 DNC C1996-137491
TI **Long** composite **solder** material for **connecting** semiconductor chip - comprises **lead** and **tin** mixed with granules, which is then plastically worked.
DC L03 M23 P55 U11 V04 X24
PA (TANF) TANAKA DENSHI KOGYO KK
CYC 1
PI JP 08215881 A 19960827 (199644)* 6p B23K035-26
ADT JP 08215881 A JP 1995-22472 19950210
PRAI JP 1995-22472 19950210
IC ICM B23K035-26
ICS B23K035-14; B23K035-40; C22C013-00
AB JP 08215881 A UPAB: 19961104
The **long** length composite **solder** material is made by mixing 0.01-5 wt% granules with a **solder** material matrix comprising 55-65 wt% Sn, and balance Pb except incidental impurities, followed by plastic working the mixture.
USE - For connecting semiconductor chips to a substrate.
Dwg.0/2
FS CPI EPI GMPI
FA AB
MC CPI: **L04-C17A**; M23-A01
EPI: U11-D03B3; V04-R04A5; X24-A01A

L124 ANSWER 18 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-162179 [17] WPIX
DNN N1996-135853 DNC C1996-051350
TI Alloy **solder** connect assembly and method - has a first alloy of lower m.pt. contacting a **compliant** second alloy of higher m.pt. which dissolves into the first on heating to form a third alloy.
DC L03 M23 P55 U11
IN BRATSCHUN, W R; LEICHT, J L; BRATSCHUN, W
PA (MOTI) MOTOROLA INC
CYC 5
PI

GB 2293564	A	19960403 (199617)*	24p	B23K035-02
DE 19536260	A1	19960411 (199620)	12p	H01L021-60
JP 08116169	A	19960507 (199628)	10p	H05K003-34
US 5551627	A	19960903 (199641)	10p	H05K003-34
SG 46949	A1	19980320 (199818)		H05K003-34
GB 2293564	B	19981202 (199850)		B23K035-02

ADT GB 2293564 A GB 1995-19222 19950920; DE 19536260 A1 DE 1995-19536260 19950928; JP 08116169 A JP 1995-274745 19950928; US 5551627 A US 1994-314833 19940929; SG 46949 A1 SG 1995-1420 19950925; GB 2293564 B GB 1995-19222 19950920
PRAI US 1994-314833 19940929
IC ICM B23K035-02; H01L021-60; H05K003-34
ICS B23K035-22; B23K035-24; B23K035-26; H01L021-58; H01L023-32
AB GB 2293564 A UPAB: 19960428
Molten alloy connection is formed to a faying surface of a substrate by: depositing a first alloy **solder** (I) having a first m.pt. on the surface; placing a second alloy **solder** (II) of **compliant** material in contact on (I), (II) having a higher m.pt. than (I); and heating to an intermediate temp. to dissolve (II) into (I) to form a third alloy **solder**. Molten alloy connection assembly interconnecting first and second faying surfaces comprises a preform (210) of (II) placed between fillets (212, 214) of (I), which has been heated to cause a region of graded compsn. between the preform and each fillet. Pref., (II) is an In **solder** alloy.
(I) is an In-free **solder**. (II) comprises 3-50 wt.% In, balance Pb; or 90-97 wt.% In, balance Ag. The difference in m.pt. between (I) and (II) is at least 25deg.C.
USE - Esp. in IC package connection structures.
ADVANTAGE - **Solder** connection is cost-effective, **compliant** and **fatigue** resistant and is able to withstand temp. induced shear stress.
Dwg.2/5
ABEQ US 5551627 A UPAB: 19961011
A method of forming a melted alloy connection to a faying surface of a substrate, the method comprising the steps of:
(a) depositing a first alloy **solder** having a first melting point onto the faying surface;
(b) placing a second alloy **solder** formed of a material more **compliant** than the first alloy **solder** in contact with the first alloy **solder**, the second alloy **solder** having a second melting point greater than the first melting point; and
(c) heating the first alloy **solder** and the second alloy **solder** to a temperature between the first melting point and the second melting point sufficient to dissolve the material more **compliant** than the first alloy **solder** from the second alloy **solder** into the first alloy **solder** and transform the first alloy **solder** into a third alloy **solder** that is elementally different from the first alloy **solder**.
Dwg.5/5
FS CPI EPI GMPI
FA AB; GI

L124 ANSWER 22 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1994-069826 [09] WPIX
DNN N1994-054698
TI Multi-chip module for small mounting area - uses **soldering**-bump for longitudinal connection of IC chip's, and connections among chip electrons and between electrode and pad on dielectric-substrate, eliminating need of wire NoAbstract.
DC U11 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 06021327 A 19940128 (199409)* 4p H01L025-04
ADT JP 06021327 A JP 1992-173937 19920701
PRAI JP 1992-173937 19920701
IC ICM H01L025-04
ICS **H01L023-52**; H01L025-18
AB JP 06021327 A UPAB: 19940418
Dwg.1/2
FS EPI
FA AB; GI
MC EPI: U11-D01A6; U11-D03C3; U14-H03A4

L124 ANSWER 23 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1993-337209 [42] WPIX
DNN N1993-260600
TI Forming electrical connection between electrical wires and cables - using heat recoverable sleeve to retain wires in thermal **contact** with conical spring and **solder** insert.
DC V04 X24
IN BRIENS, S; DELALLE, J; LAMOME, A
PA (RAYC) RAYCHEM LTD; (RAYC) RAYCHEM NV SA
CYC 21
PI WO 9320596 A1 19931014 (199342)* 26p H01R004-72
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: CA JP MG US
EP 634059 A1 19950118 (199507) EN 2p H01R004-72
R: AT BE CH DE DK ES FR GB IT LI NL SE
JP 07505254 W 19950608 (199531) 7p H01R004-72
US 5579575 A 19961203 (199703) 9p H01R043-02
EP 634059 B1 19990512 (199923) EN H01R004-72
R: AT BE CH DE DK ES FR GB IT LI NL SE
DE 69324913 E 19990617 (199930) H01R004-72
ADT WO 9320596 A1 WO 1993-GB658 19930330; EP 634059 A1 EP 1993-907950 19930330, WO 1993-GB658 19930330; JP 07505254 W JP 1993-517228 19930330, WO 1993-GB658 19930330; US 5579575 A WO 1993-GB658 19930330, US 1994-307727 19940923; EP 634059 B1 EP 1993-907950 19930330, WO 1993-GB658 19930330; DE 69324913 E DE 1993-624913 19930330, EP 1993-907950 19930330, WO 1993-GB658 19930330
FDT EP 634059 A1 Based on WO 9320596; JP 07505254 W Based on WO 9320596; US 5579575 A Based on WO 9320596; EP 634059 B1 Based on WO 9320596; DE 69324913 E Based on EP 634059, Based on WO 9320596
PRAI GB 1992-7174 19920401
REP EP 371458; WO 9200616
IC ICM H01R004-72; H01R043-02
ICS H05B003-02
AB WO 9320596 A UPAB: 19931202
A dimensionally heat-recoverable sleeve (3) is formed from cross-linked and expanded polvinylidine fluoride, and a connecting element (4) formed as a frusto-conical spring of low carbon steel. A ring (8) of a **Pb -Sn** eutectic **solder** is located about the external surface of the connecting element.
In forming an electrical connection, wires (2) in a bundle, are striped of insulation and inserted into the open end of the connector (1) until they abut an end stop, and then twisted into the connecting element. The wires and connector are inserted into an induction heating coil (12), causing the **solder** ring to melt and flow, forming a **solder** bond between wires and connecting element.
ADVANTAGE - Allows correct amount of heat to be applied to

solder to melt it, and to sleeve to cause recovery without overheating problems.
Dwg.2/7
ABEQ US 5579575 A UPAB: 19970115
A method of forming a **solder** connection between a plurality of **elongate** bodies, which comprises:
(i) forming an initial connection between the **elongate** bodies by inserting them into an induction heatable connecting element of a connector, the connector comprising a dimensionally heat-recoverable sleeve and, retained within the sleeve, the connecting element and a **solder** insert that is in thermal **contact** with the connecting element; and
(ii) heating the connector (a) by subjecting the connecting element to an alternating magnetic field so that it is heated by induction thereby melting the **solder** insert, and (b) simultaneously subjecting the sleeve to at least one of hot air and infrared radiation, thereby causing the sleeve to recover.
Dwg.2/7
FS EPI

L121 ANSWER 6 OF 9 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1996-286507 [29] WPIX
DNN N1996-240535 DNC C1996-091620
TI Structure formed with moulded plastic package for integrated circuit die - comprises semiconductor die, wire bonded at attachment point to surface of semiconductor die and layer of stress relief material.
DC A85 L03 U11
IN SHU, W K
PA (VLSI-N) VLSI TECHNOLOGY INC
CYC 1
PI US 5525839 A 19960611 (199629)* 6p H01L023-48
ADT US 5525839 A US 1994-366699 19941230
PRAI US 1994-366699 19941230
IC ICM H01L023-48
ICS **H01L023-52**
AB US 5525839 A UPAB: 19960724
The structure formed within moulded plastic package comprises a semi-conductor die (10) having a wire (16) bonded to its surface (24) at an attachment point (12), the wire forming a bond ball (17) at the attachment point having a neck (19) with enlarged metallic grains. A layer of stress relief material (26) covers the entire surface of the semiconductor die including the area where the bond ball is attached at the attachment point but it does not cover the enlarged metallic grains of the neck of the bond ball.

USE - Used for packaging of an integrated circuit in a moulded plastic package after forming a coating of stress relief material on its surface to prevent it from cracking because of a **thermal expansion** mismatch between it and the moulding cpd..

ADVANTAGE - Because the layer of stress relief material is kept below the ball neck area where the wires are bonded to the die, shearing forces resulting from **thermal expansion** at the surface interface between the layer and the plastic mould material, are less likely to cut the bond wires. Also, because the height of the layer is lower, the thickness of the plastic mould material can be increased to maximise the mechanical strength and integrity of the package. Also, the thinner layer acts as a **decoupling** layer separating the surface of the die from the moulding cpd. It prevents the moulding cpd. from adhering to the die surface and maximises the strength and integrity of the package.

Dwg.3/4
FS CPI EPI
FA AB; GI
MC CPI: A06-A00E2; A12-E04; A12-E07C; L04-F05
EPI: U11-D01A1; U11-D03A1; U11-E02A3
PLE UPA 19960823
[1.1] 018; P1445-R F81 Si 4A; S9999 S1434
[1.2] 018; ND01; Q9999 Q7476 Q7330; Q9999 Q7523; B9999 B3838-R B3747; N9999 N7170 N7023; B9999 B5538 B5505; K9676-R; K9483-R; B9999 B3861 B3849 B3838 B3747; B9999 B5243-R B4740; B9999 B4091-R B3838 B3747
[1.3] 018; A999 A351 A340; S9999 S1376
[2.1] 018; A999 A782; A999 A351 A340; S9999 S1376; P1445-R F81 Si 4A

L124 ANSWER 20 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1994-210101 [26] WPIX
DNN N1994-165482 DNC C1994-096038
TI Triazine polymer prepd. by reacting mono cyanate and di cyanate or its prepolymers - useful in thermally stable compsns. for sealing a **soldered** joint between a semiconductor device and a substrate with enhanced **fatigue** life.
DC A26 A85 L03 U11 V04
IN PAPTHOMAS, K I; PAPATHOMAS, K I
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI EP 604823 A1 19940706 (199426)* EN 13p C08G073-06
R: DE FR GB
JP 06228308 A 19940816 (199437) 8p C08G073-06
US 5468790 A 19951121 (199601) 9p C08K005-34
US 5536765 A 19960716 (199634) 9p C08K005-34
US 5623006 A 19970422 (199722) 9p C08K005-34
AB EP 604823 A UPAB: 19940817
A triazine polymer comprises a reaction prod. of (a) monocyanate; and (b) dicyanate and/or prepolymers thereof.

Also claimed are:

(1) compsn. contg. 30-50 wt.% above polymer, 50-70 (55) wt.% filler having max. particle size 49 micron and substantially free of alpha particle emissions, and opt. 0.5-3 (1-1.4) wt.% surfactant selected from silanes and non-ionic surface active agents, pref. a non-ionic alkylphenyl polyether alcohol;

(2) a **solder** interconnection for forming connections between an integrated semiconductor device and a carrier substrate comprising a plurality of **solder** connections extending from, and forming a gap between them, the gap being filled with a compsn. obtained by curing compsn. (1); and

(3) sealing a **soldered** joint between a semiconductor device and a substrate comprising (a) injecting a thermosetting compsn. (1) into a gap between the integrated circuit chip and substrate; and (b) curing the dicyanate and monocyanate forming a triazine.

The polymer is pref. made from 5-50 (5-40) wt.% (a) and 50-95 (60-95) wt.% (b). (a) is nonylphenyl, dinonylphenyl and/or cumyl phenyl cyanate. (b) is 4,4'-ethylidene bisphenol dicyanate.

The compsn. has viscosity (25 deg.C) 2000-20,000 centipoise. The filler is an inorganic filler selected from silica, quartz and fused silica coated with coupling agents. It has an emission rate of less than 0.005 alpha particles/cm2.hr. and particle sizes 0.5 49 micron. The compsn. is free of unreactive organic solvents. It may further include a catalyst.

The substrate carrier is a ceramic, FR-4 epoxy, epoxy-glass reinforced substrate, polyimide **flexible** substrate or thermoplastic substrate.

The gap is 50-150 micron (2-6 mils) wide.

USE/ADVANTAGE - The compsns. are useful for sealing a **soldered** joint between a semiconductor device and substrate (claimed), esp. for enhancing **fatigue** life of the C4 **solder** connections of an integrated semiconductor device on a substrate. The compsns. are curable at relatively low temps. (below 200 deg.C), and exhibit excellent thermal stability and relatively low **thermal expansion** coefficients. Prior to curing they have relatively low viscosity resulting in even and adequate flow under the semiconductor device.

Dwg.1/2
ABEQ US 5468790 A UPAB: 19960108
A compsn. contains a triazine polymer comprising a reaction prod. of (a) monocyanate; and (b) dicyanate, prepolymers or mixts. thereof, the amt. of (a) being 5-50 wt.% of the total of (a) and (b) and the amt. of (b) being 50-95 wt.% based on the amount of (a) and (b); and filler having a max. particle size of 49 microns and being substantially free of alpha particle emissions. The amt. of the polymer is 30-50 wt.% of the total of polymer and filler and the amount of filler is 50-70 wt.% based on the wt. of polymer and filler.

Dwg.0/2
ABEQ US 5536765 A UPAB: 19960829
A method of sealing a **soldered** joint between a semiconductor device and a substrate comprising the steps of: a) injecting a thermosetting composition contg. as binder (1) a monomeric dicyanate and (2) a monomeric monocyanate into a gap located between the integrated circuit chip and the substrate, where the amt. of (2) is about 5 to about 50% by wt. of the total of (1) and (2), and correspondingly, the amt. of (1) is about 50% to about 95% by wt. based upon the amt. of (1) and (2); and where the composition further comprises filler having a max. particle size of about 49 microns and being free of alpha particle emissions; where the amt. of the binder is about 30% to about 50% by wt. of the total of binder and filler and correspondingly, the amt. of filler is about 50% to about 70% by wt. based upon the wt. of polymer and filler; and b) curing the dicyanate and monocyanate to form a triazine.
Dwg.1/2
ABEQ US 5623006 A UPAB: 19970530
A **solder** interconnection for forming connections between an integrated semiconductor device and a carrier substrate comprising:
a number of **solder** connections that extend from the carrier substrate to electrodes on the semiconductor device to form a gap between the carrier substrate and the semiconductor device, where the gap is filled with a composition obtained from curing a composition containing as binder:
(a) monocyanate; and
(b) dicyanate; prepolymer of it or mixtures of it, where the amount of (a) is about 5 to about 50% by weight of the total of (a) and (b), and correspondingly, the amount of (b) is about 50% to about 95% by weight based upon the amount of (a) and (b), and filler having a maximum particle size of about 49 microns and being free of alpha particle emissions; where the amount of the polymer is about 30% to about 50% by weight of the total of polymer and filler and correspondingly, the amount of filler is about 50% to about 70% by weight based upon the weight of polymer and filler.
Dwg.1/2
FS CPI EPI
FA AB
MC CPI: A05-J02; A08-R01; A11-C02; A12-E04; A12-E07C; L04-C17; L04-F01; L04-F02

L124 ANSWER 19 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1995-292325 [38] WPIX
DNN N1995-221118
TI SMD type electrical lead and clip structure for substrates - has **elongated** flat strip of conductive resilient material, the strip having a U-shaped configuration adjacent to one end.
DC V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES
CYC 64
PI US 5441430 A 19950815 (199538)* 8p H01R004-02
WO 9528017 A1 19951019 (199547) EN 18p H01R004-02
AU 9522076 A 19951030 (199606) H01R004-02
EP 754356 A1 19970122 (199709) EN 8p H01R004-02
R: DE FR GB
EP 754356 B1 20030226 (200316) EN H01R012-04
R: DE FR GB
DE 69529741 E 20030403 (200330) H01R012-04
AB US 5441430 A UPAB: 19950927
A lead having a clip and terminal comprises an **elongated** flat strip of conductive resilient material, the strip having adjacent one end a U-shaped configuration with first and second parallel side arms and a joining section forming a clip, and at least one side arm carrying a **solder mass** on its side facing the other side arm. The clip is adapted to engage a first substrate having a contact pad in register with the **solder mass**.

The strip has a first straight section joined to the clip first arm and folded to be parallel to the clip arms, the strip having a terminal straight section at right angles to the first section and to the clip arms, and adapted to be surface-mounted on a second substrate. The terminal straight section is longer than the clip-joining section and extends beyond the clip on either side of the clip.

USE/ADVANTAGE - For surface-mounting a first substrate perpendicularly to a second substrate. Reduces the effects of shock and vibration. Enhances stability of lead during and after mounting it on PCB.
Dwg.5/8
FS EPI

L124 ANSWER 28 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-152171 [19] WPIX
DNN N1992-113519 DNC C1992-070351
TI Removable VLSI **package** - includes contact pins with matching cavities filled with conductive material and covered with foil.
DC A85 L03 U11
IN BLUM, A; GERTH, F; PERSKE, M; SCHMIDT, M
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 5
PI EP 483408 A 19920506 (199219)* EN 7p
R: DE FR GB
US 5164818 A 19921117 (199249) 5p H01L023-02
JP 05003052 A 19930108 (199306) 5p H01R004-02
EP 483408 B1 19950208 (199510) EN 6p H05K003-32
R: DE FR GB
DE 69016785 E 19950323 (199517) H05K003-32
AB EP 483408 A UPAB: 19931006
Removable package of at least one device (1) and a wiring substrate (5) comprises: at least one plug-in pin (2) on the surface of the device or substrate: at least one corresponding cavity (3) to receive the pin; conductive material (7) in the cavity; and a foil (4) covering the cavity and sealing the material. The pin pierces the foil, making contact with the conductive material.
The pin is pref. made of, or coated with, W, WC, Cu-Be or doped Si.
USE/ADVANTAGE - Esp. with a high density packaging system for VLSI devices. System is easily assembled and disassembled and has high resistance to **temp. cycling stress**. (3/4)
3/4
ABEQ US 5164818 A UPAB: 19931006
The removable VLS1 assembly comprises (a) several **elongated** means on the device surface and extending perpendicular to its major surface, (b) a substrate with cavities on its major surface, each cavity located w.r.t. the corresp. position of one of the **elongated** means, (c) a conductive metal with m.pt. no greater than wood alloy m.pts. in each cavity, and (d) a nonconductive foil covering each cavity and conductive metal. The **elongated** means are tapered contact pins formed from W, WC, Cu-Be or doped Si, by etching and are about 30 microns in dia. and have a tip sharpened to about 5 microns. The cavities are connected to wiring on the substrate.
USE/ADVANTAGE - Easy assembly/disassembly of high density interconnections. The assembly has high resistance to **temp. cycle stresses**, thus enhancing stability and lifetime.
Used in multilayer TAB applications.
3/4
ABEQ EP 483408 B UPAB: 19950314
A removable package of at least one electronic device (1) and a wiring substrate (5), comprising at least one pin (2) located on the surface (11) of said electronic device or on the surface (12) of said substrate (5), at least one cavity (3) on the surface (12) of said substrate or on the surface (11) of said device, respectively, located with respect to the corresponding positions of said pin, a low melting point alloy or mercury (7), provided in said cavity and a non-conductive foil (4), covering said cavity and sealing said low melting point alloy or mercury, characterised in that said foil (4) is elastic and penetrated by said pin (2) thus causing electrical contact between said low melting point alloy (7) or mercury, and said pin (2), whereby said foil (4) has a thickness less or equal to the diameter of the opening (13) caused by said penetration of said pin (2).
Dwg.1-4/4
FS CPI EPI
FA AB; GI
MC CPI: A12-E07C; A12-P; L03-H04E9; L04-C20D; **L04-C21**; L04-F05
EPI: U11-D03A3; U11-D03A9; U11-E01X
PLC UPA 19930924
KS: 0209 0231 0759 1291 2551 2774

L124 ANSWER 51 OF 53 JAPIO (C) 2003 JPO on STN
AN 1998-163413 JAPIO
TI **MICROELECTRONIC PACKAGING** USING ARCHED **SOLDER COLUMNS**
IN RINNE GLENN A; DEANE PHILIP A
PA MCNC
PI JP 10163413 A 19980619 Heisei
AI JP 1997-138944 (JP09138944 Heisei) 19970528
PRAI US 1996-654539 19960529
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
IC ICM H01L025-00
ICS H05K001-14; H05K003-36
AB PROBLEM TO BE SOLVED: To provide a solid microelectronic package and a method for manufacturing the package.
SOLUTION: In the method for manufacturing a microelectronic package, **solder** bumps provided on one or more substrates are expanded to be extended to another substrate and to contacted with it, forming a **solder** connection therewith. Expansion of the **solder** bump is carried out preferably by reflowing additional **solder** to a plurality of **solder** bumps. The additional **solder** reflows from an **elongated** narrow **solder**-containing region 206 adjacent to the **solder** bump into a **solder** bump 310a (312). After reflow, a **solder** bump 310b which extends across a pair of adjacent substrates 100 and 200 forms a single arched **solder column** or partial ring 320 between the two substrates.

L124 ANSWER 50 OF 53 JAPIO (C) 2003 JPO on STN
AN 1999-135673 JAPIO
TI WIRING BOARD AND **INTERCONNECTION** BOARD
IN MORI KOICHI
PA NGK SPARK PLUG CO LTD
PI JP 11135673 A 19990521 Heisei
AI JP 1997-296043 (JP09296043 Heisei) 19971028
PRAI JP 1997-296043 **19971028**
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
IC ICM H01L023-12
ICS H01L021-60; H01L023-32; H01L023-50
AB PROBLEM TO BE SOLVED: To provide a wiring board having higher reliability of connection with a fixing board or an interconnection board with higher reliability of connection with the wiring board or the fixing board.
SOLUTION: This wiring board 10 comprises an alumina ceramic wiring board body 1, having first and second faces 1a, 1b, a terminal pad 2 formed on the second faces 1b side, and a **columnar** terminals 3 for connection with a printed board (fixing board 20. The terminal 3 is bonded to the terminal **pad** 2 and composed of a high temperature **solder**, having a hemispherical forward end part 3a to be connected with the printed board, a base end part 3c to be bonded to the terminal pad 2, and a **columnar** part 3b **elongated** axially longer than the diameter thereof and interposed between the forward end part 3a and the base end part 3c. The base end part 3c has a diameter increasing gradually from the **columnar** part 3b toward the terminal pad 2.
Even if deformation takes place due to the **difference** of **thermal expansion** between the wiring board 10 the printed board 20, the **columnar** part 3b of the terminals 3 is bent, and the base end part 3c prevents concentration of stresses. Consequently, the board is tends not to rupture and high connection reliability can be attained.
COPYRIGHT: (C)1999,JPO

L124 ANSWER 44 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1986-205916 [32] WPIX
DNN N1986-153627 DNC C1986-088460
TI **Solder interconnection** between integrated semiconductor and substrate - having array of **solder** connections with organic dielectric material embedding outer row(s) of connections.
DC A85 L03 M23 U11 U14
IN BECKHAM, K F; KOLMAN, A E; MCGUIRE, K M; PUTTLITZ, K J; QUINONES, H
PA (IBMC) IBM CORP
CYC 7
PI EP 189791 A 19860806 (198632)* EN 22p
R: DE FR GB IT
US 4604644 A 19860805 (198634)
JP 61177738 A 19860809 (198638)
CA 1224576 A 19870721 (198733)
EP 189791 B 19901114 (199046)
R: DE FR GB IT
DE 3675554 G 19901220 (199101)
ADT EP 189791 A EP 1986-100553 19860117; US 4604644 A US 1985-695597 19850128; JP 61177738 A JP 1985-204604 19850918
PRAI US 1985-695597 19850128
REP 2.Jnl.Ref; A3...8745; DE 2736090; FR 2124488; JP 59106140; No-SR.Pub; US 3719981; US 4381602
IC H01L021-60; H01L023-50; H05K003-34; H05K007-06
AB EP 189791 A UPAB: 19930922
A **solder** interconnection for forming I/O connections between an integrated semiconductor device and a support substrate comprises several **solder** connections arranged in an area array joining a set of I/O's on a flat surface of the semiconductor device to a corresponding set of **solder** wettable **pads** on a substrate, and a band of dielectric organic material disposed between and bonded to the device and substrate embedding at least an outer row of **solder** connections, and leaving the central inner **solder** connections and the adjacent top and bottom surface free of dielectric material.

Pref. the band of dielectric material covers as a min. a single outer peripheral row and **column**, and as a max. the rows and **columns** outside the line where the normal axial displacement of the **solder** terminals is zero when no dielectric material is present. The band of dielectric material is pref. of a polyamide-imide polymer formed by reacting the cpd. (I) with trimellitic anhydride or acyl chloride of trimellitic anhydride and further reacting the prod. with aminopropyl triethoxy silane or beta-(3,4-epoxycyclohexyl) ethyltrimethoxy silane.

USE/ADVANTAGE - The process is useful for joining a micro-miniaturised component to a supporting board or substrate and gives a **solder** bond structure with increased **fatigue** life.

0/6
ABEQ EP 189791 B UPAB: 19930922
An improved **solder** interconnection for forming I/O connections between an integrated semiconductor device and a support substrate comprising a plurality of **solder** connections (13) arranged in an area array joining a set of I/Os on a flat surface of said semiconductor device to a corresponding set of **solder** wettable **pads** on a substrate characterised by a band of dielectric organic material (30) disposed between and bonded to said device (10) and substrate (12) embedding at least an outer row of **solder** connections, and leaving the central inner **solder** connections and the adjacent top and bottom surfaces free of dielectric material, wherein said band of dielectric material covers as a minimum a single outer peripheral row and **column**, and as a maximum the rows and **columns** outside the line where the normal axis displacement of the **solder** terminals is zero when no dielectric material is present.
ABEQ US 4604644 A UPAB: 19930922
I/O connections between integrated semiconductor devices (SCD) and a support substrate consists of A) numerous **solder** connections (SC) arranged in an area array to join a set of I/O's on a flat surface of the SCD to a corresponding set of **solder** wettable **pads**

on a substrate and B) a band of dielectric organic material (DOM) arranged between and bonded to the SCD and substrate embedding at least an outer row of SC while leaving free from the DOM the central inner SC, the central underside device surface, the opposing substrate surface as well as the top surface of the SCD.

The band of the DOM is a polyamide-imide polymer esp. formed by reacting a) P,P'-diaminodiphenyl -methane with b) mellithic anhydride or its acylchloride and then reacting the product with c) gamma-aminopropyl triethoxy silane or beta-(3,4-epoxy cyclohexyl) ethyltrimethoxy silane. The spacing between the SCD and the substrate is 2-10, esp. 2-4 mils.

ADVANTAGE - An improved **solder interconnection** structure is provided having a **longer fatigue** life than known ones; large devices can be accommodated.

FS CPI EPI
FA AB
MC CPI: A05-J01B; A11-C01A1; A12-E07; A12-E07C; **L04-C17A**; M23-A04
EPI: U11-D03; U11-E02; U14-H04B
DRN 5014-U; 5268-U
PLC UPA 19930924

L124 ANSWER 42 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1986-232037 [35] WPIX
CR 1984-036985 [06]; 1988-322269 [45]; 1990-043919 [06]; 1991-309926 [42]; 1992-299147 [36]; 1994-248193 [30]
DNN N1986-173361
TI **Solder**-bearing lead for PCB surface mounted device - has side ears formed on contact blank, and then bent upwardly to hold **solder mass** near pad.
AW MULTIPLE CONTACT CONNECT.
DC P55 S01 U14 V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES CORP
CYC 1
PI US 4605278 A 19860812 (198635)* 7p
ADT US 4605278 A US 1985-737830 19850524
PRAI US 1985-737830 19850524; US 1985-793654 19851031; US 1986-850754 19860411; US 1986-876820 19860620; US 1987-87084 19870819
IC H01R004-02
AB US 4605278 A UPAB: 19940921
A **solder**-bearing portion (30) of a lead is bent at a right angle to the remainder of a body (16). A spring finger (22) is positioned with a bend (32) opposite the **solder mass** (26). This provides a springy gap between the **solder** and the bend within which may be inserted a circuit board or other substrate (34) having a conductive area or contact pad (36).

The resilience of the finger serves to retain the lead in position on the board before the **soldering** is done, and as the **solder** melts upon application of heat, the finger allows tabs (18) to move relatively toward and into contact with the conductive area. The lead forms an edge clip for the circuit board, and the terminal end (38) of the lead may be formed in a number of ways for connection to other equipment, e.g. as a pin for insertion into a contact receptacle, or as a wire-wrapped post termination.

USE/ADVANTAGE - Also for multiple contact connectors. Lead may be manufactured by automatic progressive stamping at high speed.
Dwg.5/11
Dwg.5/11
ABEQ DE 3685872 G UPAB: 19930922
The terminal pin which is to be **soldered** into a bush (22) mounted in a hole through a printed circuit board (21) or other substrate forms one of a continuous set of pins stamped from sheet metal. Each pin has a central blade (14,15) between two rectangular section arms forming the contact ends, to which circuit connections are made. During stamping, a cut is made down each edge of the blade, forming two resilient side arms (16) which are bent back, to lock a cylindrical piece of **solder** (17) across the blade.

After the pin has been inserted, heat is applied to melt the **solder** which runs downwards and connects the pin to the bush in the board. After stamping, the pins are connected between edge strips with indexing and locating holes, to form a continuous composite strip, and each pin is connected by weak zones so that it can be easily detached from its edge strips.
ABEQ EP 223830 B UPAB: 19930922
A **solder**-bearing lead adapted to be **soldered** to a conductive surface comprising an **elongate** body portion (16) including means (18) for holding a **solder mass** on said body portion, characterised by a strip-like body portion (16) having on at least one edge thereof at least one laterally extending tab (18) each said tab being bent into a plane substantially perpendicular to the plane of said body portion for holding said **solder mass** substantially transversely of said body portion.
1/22
FS EPI GMPI

L124 ANSWER 31 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1991-309926 [42] WPIX
CR 1984-036985 [06]; 1986-232037 [35]; 1988-322269 [45]; 1990-043919 [06]; 1992-299147 [36]; 1994-248193 [30]
DNN N1991-237628
TI **Solder** bearing terminal pin and lead - has mass of **solder** held by lead near to substrate receptacle or surface in position to be melted for bonding.
DC V04 X24
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES CORP
CYC 1
PI US 5052954 A 19911001 (199142)*
ADT US 5052954 A US 1989-416505 19891003
PRAI US 1982-396764 19820709; US 1984-600362 19840416; US 1985-737830 19850524; US 1985-793654 19851031; US 1986-850754 19860411; US 1986-876820 19860620; US 1987-129715 19871207; US 1989-416505 19891003
IC H01R004-02
AB US 5052954 A UPAB: 19940921
C.i.p. 4728305, 4679889, 4605278 Continuation 4883435 (+20.06.86, 16.04.84, 11.04.86, 31.10.85, 24.05.85 -US- 876820, 600362, 850754, 793654, 737830) (1895BL)

The lead has a conductive member with an **elongated** body and a curved portion bent out of the body forming an opening on its concave side. The curved portion has an end forming a **solderable** portion for **soldering** to a substrate conductive area, and opening faces in a direction along the **elongated** body. A **solderable** portion is opposed adjacent and substantially in contact with a substrate conductive area when the lead is mated with the substrate.

A mass of **solder** (17) is carried by the conductive member within the curved portion opening and held between and directly engaging the body and curved portion. Upon mating of the lead and substrate with the conductive area adjacent the sodlerable portion, the **solder mass** is in contact with the substrate conductive area, without the curved portion being between the sodler mass and the conductive area. When the sodler is melted, the lead is connected to the substrate with an electrical and mechanical bond.

USE/ADVANTAGE - **Soldering** terminal pin or surface-mounted lead to PCB. Lead provides unobstructed flow for melted **solder**.
@(10pp Dwg.No.1/18)@(
FS EPI
FA AB; GI

L124 ANSWER 32 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1991-222107 [30] WPIX
CR 1992-088259 [11]; 1995-292324 [38]
DNN N1991-169591
TI **Solder**-bearing lead for attachment to contact pad - includes pair of projections extending from body edge, forming gap to receive **solder mass**.
DC U11 V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES; (NAMS-N) N AMER SPECIALITIES; (NASP-N) N AMER SPECIALTIES
CYC 14
PI US 5030144 A 19910709 (199130)* 9p
WO 9116736 A 19911031 (199146)
RW: AT BE CH DE DK ES FR GB GR IT LU NL SE
W: US
EP 524248 A1 19930127 (199304) EN 32p H01R004-02
R: DE ES FR GB IT NL SE
US 5344343 A 19940906 (199435)# 14p H01R004-02
EP 524248 A4 19950816 (199618)
EP 524248 B1 19991013 (199947) EN H01R004-02
R: DE ES FR GB IT NL SE
DE 69131712 E 19991118 (200001) H01R004-02
AB US 5030144 A UPAB: 20000105
The **solder**-bearing portion of the lead includes a pair of projections extending from one edge to form a gap between which is dimensioned to receive and retain a **solder mass**. A region of a portion of the lead is twisted so that the edge of the **solder**-bearing portion containing the projections is bent so that the projections lie in a plane perpendicular to the plane of the remaining portion. Since the thickness of the lead when formed is less than its width, the twisting of the **solder** bearing portion results in a lesser width of that portion adapted to contact the substrate and permits closer spacing of leads.

A **solder mass** is placed within the projections of the **solder**-bearing portion to provide electrical bonding between the lead and the substrate. The **solder**-bearing lead can be used as an edge clip for mounting a substrate or for surface mounting the substrate. The **solder**-bearing lead can be made by automatic progressive stamping of blanks at high speed and simple twisting of the lead.

Dwg.7/13
ABEQ US 5344343 A UPAB: 19941021
The **solder**-bearing lead comprises an **elongated** body portion having a **solder**-bearing portion, a terminal portion, and a middle portion disposed between the **solder**-bearing portion and the terminal portion. The **solder**-bearing portion carries a **solder mass** either on a pair of projections extending from one edge of the body portion and forming a gap inbetween dimensioned to receive a **solder mass**, or on the opposed faces of the **solderbearing** portion.

A region of the middle portion is twisted so that the **solder**-bearing portion lies in a plane perpendicular to the plane of the terminal portion.

USE - Is adapted to be **soldered** to a conductive surface.
The **solder**-bearing lead can be used as an edge clip for mounting a substrate such as printed circuit board, or as a surfacemounted lead for a substrate.
Dwg.17A/19

L124 ANSWER 33 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1991-029943 [05] WPIX
DNN N1991-023129 DNC C1991-012819
TI Protective coating for **soldered contact** of electronic device - obtd. by drying coating of non-activated flux esp. rosin soln., ethyl acetate and ethanol.
DC L03 M23 U11 U14
IN ALBRECHT, R; SCHNEIDER, U; SEIDEL, V
PA (KERH) VEB KERAMISCHE WERKE HERMSDORF
CYC 1
PI DD 282109 A 19900829 (199105)*
ADT DD 282109 A DD 1989-326015 19890224
PRAI DD 1989-326015 19890224
IC H01L021-56
AB DD 282109 A UPAB: 19930928
Protective coating for **soldered contacts** of electronic devices consists of a residue remaining on the entire device, which is applied from a soln., pref. by dipping, and dried in air at room temp.. The soln. consists of a unactivated flux, esp. a rosin soln., and a mixt. of 85 vol.% ethyl acetate and 15 mol.% EtOH in 1:50-100 vol. ratio, the film thickness being under 1 micron.
USE/ADVANTAGE - The coating is esp. useful for **soldered contacts** of thick film circuits. It inhibits corrosion, ensuring that the **contacts** remain **solderable** for **long** periods, and is not costly to produce.
0/0
FS CPI EPI
FA AB
MC CPI: L04-C11D; **L04-C17A**; M23-A02
EPI: U11-D01C; **U11-D03B**; U14-H02

L124 ANSWER 34 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1991-025923 [04] WPIX
DNN N1991-019895 DNC C1991-011125
TI **Solder** material for semiconductor device mfr. - comprises **lead**, **tin** and **copper** for improved ageing properties.
DC L03 M23 M26 P55
PA (TANI) TANAKA KIKINZOKU KOGYO KK
CYC 1
PI JP 02295699 A 19901206 (199104)*
JP 06071676 B2 19940914 (199435) 4p B23K035-26
ADT JP 02295699 A JP 1989-113977 19890506; JP 06071676 B2 JP 1989-113977 19890506
FDT JP 06071676 B2 Based on JP 02295699
PRAI JP 1989-113977 19890506
IC B23K035-26; C22C011-06
ICM B23K035-26
ICS B23K035-40; C22C011-06
AB JP 02295699 A UPAB: 19930928
Solder material comprises Pb contg. 1-10 wt.% Sn, with 0.02-1.5 wt.% **Cu** added. The material is produced by quench solidification. Also claimed is a **solder** material, which comprises 0.0015-20 wt.% Sb in addn. to the **Cu**.
USE/ADVANTAGE - Provides a **solder** suitable for **soldering** semiconductor materials, partic. having improved ageing properties by adding **Cu** and further Sb. Thus, the tensile strength of the **solder** material is maintained **longer** than the operability, and reliability is partic. improved when used in wire-bonders for forming bump electrodes.
0/4
FS CPI GMPI
FA AB
MC CPI: **L04-C17A**; M23-A01; M26-B04; M26-B04C; M26-B04T

L124 ANSWER 36 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1990-043919 [06] WPIX
CR 1984-036985 [06]; 1986-232037 [35]; 1988-322269 [45]; 1991-309926 [42]; 1992-299147 [36]; 1994-248193 [30]
DNN N1991-237628
TI **Solder**-bearing terminal pin and lead - with discrete mass of **solder** mechanically held by terminal or lead close to substrate receptacle.
DC V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALTIES
CYC 1
PI US 4883435 A 19891128 (199006)* 9p
ADT US 4883435 A US 1987-129715 19871207
PRAI US 1982-396764 19820709; US 1984-600362 19840416; US 1985-737830 19850524; US 1985-793654 19851031; US 1986-850754 19860411; US 1986-876820 19860620; US 1987-129715 19871207
IC H01R004-02
AB US 4883435 A UPAB: 19940921
An **elongated** body has an upper body portion and a lower body portion, the lower body portion being sized to fit in the substrate opening perpendicular to the substrate. The body is cut longitudinally to define a finger having a first end integral with and attached to the body, also having a free end. The finger is bent out of the plane of the body and has a portion spaced from and in opposition to the body. The finger is bent only partially around the **solder mass**, with each **solder mass** held between the finger free end body. The finger free end is wrapped only partially around the **solder mass** to leave at least a portion of the **solder mass** uncovered by the finger.

The uncovered **solder mass** portion is in a position to confront directly and to contact the substrate conductive area with the end of the finger adjacent to the conductive area but not interposed between the **solder mass** and conductive area. The body is also cut longitudinally along a second line to define a second finger, the fingers being separated by the upper body portion, both of the fingers being wrapped only partially around the **solder mass**.

USE - Mechanical attachment of **solder mass** to electrical terminal.
ABEQ DE 3685872 G UPAB: 19930928
The terminal pin which is to be **soldered** into a bush (22) mounted in a hole through a printed circuit board (21) or other substrate forms one of a continuous set of pins stamped from sheet metal. Each pin has a central blade (14,15) between two rectangular section arms forming the contact ends, to which circuit connections are made. During stamping, a cut is made down each edge of the blade, forming two resilient side arms (16) which are bent back, to lock a cylindrical piece of **solder** (17) across the blade.

After the pin has been inserted, heat is applied to melt the **solder** which runs downwards and connects the pin to the bush in the board. After stamping, the pins are connected between edge strips with indexing and locating holes, to form a continuous composite strip, and each pin is connected by weak zones so that it can be easily detached from its edge strips.
ABEQ EP 223830 B UPAB: 19930928
A **solder**-bearing lead adapted to be **soldered** to a conductive surface comprising an **elongate** body portion (16) including means (18) for holding a **solder mass** on said body portion, characterised by a strip-like body portion (16) having on at least one edge thereof at least one laterally extending tab (18) each said tab being bent into a plane substantially perpendicular to the plane of said body portion for holding said **solder mass** substantially transversely of said body portion.
1/22
FS EPI
FA AB; GI

L124 ANSWER 40 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1988-322269 [45] WPIX
CR 1984-036985 [06]; 1986-232037 [35]; 1990-043919 [06]; 1991-309926 [42]; 1992-299147 [36]; 1994-248193 [30]
DNN N1988-244515
TI Conductive lead esp. for high density PCB or integrated circuit - comprises **elongate** flat conductive strip with opposed arms.
DC S01 U14 V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALTIES; (NASP-N) NORTH AMERICAN SPECIALTIES
CYC 1
PI US 4780098 A 19881025 (198845)* 12p
ADT US 4780098 A US 1987-87084 19870819
PRAI US 1982-336924 19820104; US 1985-737830 19850524; US 1985-793850 19851031; US 1986-850754 19860411; US 1987-87084 19870819
REP A3...9028; No-SR.Pub; US 4433892; US 4605278
IC H01R004-02; H01R009-09
ICM H01R009-09
ICS H01R004-02
AB US 4780098 A UPAB: 19940921
An **elongated** conductive body formed from a flat strip of resilient material, having a pair of opposed arms adapted to engage the opposed device surfaces resiliently. One of the arms carries a conductive **solder** element adapted to contact a conductive area on the first of the surfaces. A non-conductive element is held by the other of the arms, adapted to engage the second of the surfaces to insulate the lead from the second surface.

The conductive area of the second surface is insulated by the lead and the non-conductive element from the conductive area of the first surface. The body comprises a tab integral with the body and extending perpendicular to the body strip, the tab engaging and assisting in retaining the non-conductive element in a position to be fixedly opposed to the second surface of the device.

USE - Lead connection for integrated circuit, PCB or ceramic chip carrier. Also for testing PCB circuitry.

Dwg.1/10
Dwg.1/10
ABEQ DE 3685872 G UPAB: 19930923
The terminal pin which is to be **soldered** into a bush (22) mounted in a hole through a printed circuit board (21) or other substrate forms one of a continuous set of pins stamped from sheet metal. Each pin has a central blade (14,15) between two rectangular section arms forming the contact ends, to which circuit connections are made. During stamping, a cut is made down each edge of the blade, forming two resilient side arms (16) which are bent back, to lock a cylindrical piece of **solder** (17) across the blade.

After the pin has been inserted, heat is applied to melt the **solder** which runs downwards and connects the pin to the bush in the board. After stamping, the pins are connected between edge strips with indexing and locating holes, to form a continuous composite strip, and each pin is connected by weak zones so that it can be easily detached from its edge strips.
ABEQ EP 223830 B UPAB: 19930923
A **solder**-bearing lead adapted to be **soldered** to a conductive surface comprising an **elongate** body portion (16) including means (18) for holding a **solder mass** on said body portion, characterised by a strip-like body portion (16) having on at least one edge thereof at least one laterally extending tab (18) each said tab being bent into a plane substantially perpendicular to the plane of said body portion for holding said **solder mass** substantially transversely of said body portion.
1/22
ABEQ EP 303873 B UPAB: 19940209
A conductive lead (10, 210, 310) for connection to one conductive area (62, 64, 262, 264, 262', 264, 362, 364, 362', 264') of a device (60, 260, 260', 360, 361) having two opposed surfaces, said lead comprising: an **elongated** conductive body (16, 316) formed from a substantially

flat strip of resilient material and having a pair of opposed arms, (12, 13, 320, 321, 320', 321') adapted to engage said opposed device surfaces resiliently, one of said arms carrying a **solder** element (26, 226, 226', 326, 326') adapted to contact one of said conductive areas on one of said surfaces, characterised by a non-conductive element (50, 250, 250'. 350, 350') held by the other of said arms and adapted to engage an other of said surfaces also provided with an conductive area to insulate said lead (10, 210, 310) from said other surface, whereby the conductive area of sai

d other surface is insulated by said lead and said non-conductive element from the conductive area of said one surface.

Dwg.1/10

L124 ANSWER 41 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1986-332176 [50] WPIX
CR 1984-036985 [06]; 1986-232037 [35]; 1988-042611 [06]; 1988-322269 [45]; 1990-043919 [06]; 1991-309926 [42]; 1992-299147 [36]
DNN N1986-247778
TI **Solder** bearing lead for conductive surface - has blank with main body portion and side pass extending laterally.
DC P55 V04
IN SEIDLER, J
PA (NASP-N) NORTH AMERICAN SPECIALITIES; (NASP-N) NORTH AMERICAN SPECIALITIES CORP
CYC 17
PI WO 8607198 A 19861204 (198650)* EN 29p
RW: AT BE CH DE FR GB IT LU NL SE
W: AU JP KR
AU 8659512 A 19861224 (198710)
EP 223830 A 19870603 (198722) EN
R: AT BE CH DE FR GB IT LI LU NL SE
US 4679889 A 19870714 (198730)
JP 62502926 W 19871119 (198801)
US 4728305 A 19880301 (198812)
CA 1260098 A 19890926 (198944) H01R004-02
EP 223830 B1 19920701 (199227) EN 18p H01R004-02
R: AT BE CH DE FR GB IT LI LU NL SE
DE 3685872 G 19920806 (199233) H01R004-02
ADT WO 8607198 A WO 1986-US1080 19860515; EP 223830 A EP 1986-903845 19860515; US 4679889 A US 1985-793654 19851031; JP 62502926 W JP 1986-503064 19860515; US 4728305 A US 1986-850754 19860411; CA 1260098 A DE 1986-3685872 19860515, EP 1986-903845 19860515, WO 1986-US1080 19860515; EP 223830 B1 EP 1986-903845 19860515, WO 1986-US1080 19860515; DE 3685872 G DE 1986-3685872 19860515, EP 1986-903845 19860515, WO 1986-US1080 19860515
FDT CA 1260098 A Based on EP 223830, Based on WO 8607198; EP 223830 B1 Based on WO 8607198; DE 3685872 G Based on EP 223830, Based on WO 8607198
PRAI US 1985-737830 19850524; US 1985-793654 19851031; US 1986-850754 19860411; US 1986-876820 19860620; US 1987-87084 19870819
REP DE 2321828; EP 88582; SSR871021; US 4423920; US 4439000; US 4482197; US 4500149; US 4502745; US 4503609; US 4537461; US 4541034; DE 2231828
IC ICM H01R004-02
ICS H01R009-09; H01R011-22; H01R043-02
AB WO 8607198 A UPAB: 19940303
The **solder** bearing lead includes an integral, **elongated**, strip-like, planar body portion (16) having on at least one edge at least one laterally extending integral (18)tab. Each tab is bent into a plane perpendicular to the plane of the body portion and a **solder mass** (26) is held by the tab against the body portion. Each tab is bent inwardly to retain the **solder mass**.

The tabs areformed in pairs to retain the **solder mass** between them, or are in the form of single fingers partially encircling or staked to a **solder mass**. The **solder mass** is positioned to facilitate **soldering** of a terminal of a device to a substrate as for surface mounted devices.

Dwg.4,5/22

ABEQ DE 3685872 G UPAB: 19930922
The terminal pin which is to be **soldered** into a bush (22) mounted in a hole through a printed circuit board (21) or other substrate forms one of a continuous set of pins stamped from sheet metal. Each pin has a central blade (14,15) between two rectangular section arms forming the contact ends, to which circuit connections are made. During stamping, a cut is made down each edge of the blade, forming two resilient side arms (16) which are bent back, to lock a cylindrical piece of **solder** (17) across the blade.

After the pin has been inserted, heat is applied to melt the **solder** which runs downwards and connects the pin to the bush in the board. After stamping, the pins are connected between edge strips

with indexing and locating holes, to form a continuous composite strip, and each pin is connected by weak zones so that it can be easily detached from its edge strips.

ABEQ EP 223830 B UPAB: 19930922

A **solder**-bearing lead adapted to be **soldered** to a conductive surface comprising an **elongate** body portion (16) including means (18) for holding a **solder mass** on said body portion, characterised by a strip-like body portion (16) having on at least one edge thereof at least one laterally extending tab (18) each said tab being bent into a plane substantially perpendicular to the plane of said body portion for holding said **solder mass** substantially transversely of said body portion.

1/22

ABEQ US 4679889 A UPAB: 19930922

An **elongate** strip body has on at least one edge a pair of spaced laterally extending tabs defining an opening. The tabs perpendicular from the body portion strip to form, inbetween, part of a channel with said body portion forming a floor for the channel. A **solder mass** in the channel is bordered by the tabs. Thetabs are bent inwardly of the channel to retain the **solder mass**.

The **solder mass** has a dimension extending away from the body at least as great as the extent of the tabs, so that the mass extends flush of outwardly from the channel and may be placed in direct contact with the conductive surface to which the lead is to be **soldered**, while spacing the tabs from the surface. Upon melting the mass, the tabs are permitted to be or move into contact with the conductive surface to make electrical contact and to be retained in such contact upon re-solidification of the mass.

ABEQ US 4728305 A UPAB: 19930922

A **solder**-bearing terminal is formed from a blank having a main body portion and side tabs extending laterally from it, which are bent perpendicularly to the main body. The tabs may be formed in pairs to retain a **solder mass** between, or may be in the form of single fingers partially encircling or stacked to a **solder mass**.

The **solder mass** is positioned to facilitate **soldering** of a terminal of a device to a substrate, as for surface mounted devices. The tabs may be on one or both edges of the main terminal body.

USE - For use with multiple contact connectors and electronic circuit boards.

L124 ANSWER 47 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1983-10050K [05] WPIX
DNN N1983-019068 DNC C1983-009831
TI Electric connector straps for semiconductor device - where one end of strap is **soldered** to conductor path on carrier substrate, and other end is **soldered** to main or gate **contact** on device.
AW COPPER NICKEL.
DC L03 U11
IN AKYUEREK, A; HETTMANN, H; NEIDIG, A
PA (BROV) BBC BROWN BOVERI & CIE AG
CYC 9
PI EP 69903 A 19830119 (198305)* DE 10p
R: AT FR GB IT NL SE
DE 3127458 A 19830203 (198306)
JP 58070563 A 19830427 (198323)
US 4502750 A 19850305 (198512)
EP 69903 B 19861015 (198642) DE
R: AT FR GB IT NL SE
DE 3127458 C 19870625 (198725)
JP 63062096 B 19881201 (198901)
ADT EP 69903 A EP 1982-105680 19820626; DE 3127458 A DE 1981-3127458 19810711; JP 58070563 A JP 1982-119197 19820710; US 4502750 A US 1982-396652 19820809
PRAI DE 1981-3127458 19810711
REP DE 2728330; No-SR.Pub
IC H01L021-60; H01L023-48; H01L029-74; H01R004-02
AB EP 69903 A UPAB: 19930925
Each strap has bent ends terminating in **soldering**- lugs or -rings; and near the lugs employed to **solder** the straps to the conductor paths are side fins used for accurate location of the straps in a die during the **soldering** operation. A **long** thin strap is pref. used to **solder** the gate **contact** of a semiconductor device to a conductor path; whereas a short wide strap is pref. used to connect the cathode contact on the device to another conductor path. The straps are pref. made of Cu; brass; Ni-alloys; Ni or bronze. The ends of the straps are pref. coated with **solder**, or with a material which can be **soldered**, esp. Ni obtd. by chemical- or electro-plating.
The connector straps and the semiconductor device can be accurately aligned w.r.t. each other in a die or jig employed while the straps are **soldered** to the device and to the conductor paths.
1/3
ABEQ DE 3127458 C UPAB: 19930925
Connection members for a semi-conductor of a main **contact** to a conducting track, have bowed shaped section with **solder** points at the ends. The bowed section has side members which lie in a plane which is perpendicular to the **solder** points. The side members are attached between the curved sections of the section.
ADVANTAGE - The connection members enable precise electrical connections to be achieved.
ABEQ EP 69903 B UPAB: 19930925
Connecting lug for a semiconductor component for electrically connecting a main or control contact of the semiconductor component to a conductor track, in which arrangement the connecting lug consists of a strap having **solder** tabs or **solder** rings which are doubly angled at both ends, characterised in that the strap (12,16) of the connecting lug (9,10) has side wings (13,17) which are arranged between the angles of the strap (12,16) to the **solder** tab (14,18) used as connection to the conductor track (2,4).
ABEQ US 4502750 A UPAB: 19930925
Semiconductor component electrical connecting strap (10) comprises a bracket (12) with two sides and two doubly bent ends. There are **soldering** lugs (8) integral with the ends and lateral wings (13) are integral with one of the ends. The wings are spaced from a conductor run and extend transversely from the sides for positioning the strp for connection to the conductor run.

Pref. the **soldering** lugs are ring shaped and the bracket is **long** and narrow for **connection** to the gate contact of a semiconductor component.

ADVANTAGE - Accurate adjustment between the strap and semiconductor component in a **soldering** fixture is possible.

FS CPI EPI
FA AB
MC CPI: L03-D03F
EPI: **U11-D03B**

L124 ANSWER 29 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-024644 [03] WPIX
TI **Elongated solder interconnection** -
comprising a **solder mass** encapsulated by electrically conductive material and capped with a second **solder mass**

DC L03 U11 U14
IN AGARWALA, B N; AHSAN, A M; BROSS, A; CHADURJIAN, M F; KOOPMAN, N G; LEE, L; PUTTLITZ, K J; RAY, S K; RYAN, J G; SCHAEFER, J G; SRIVASTAVA, K K; TOTTA, P A; WALTON, E G; WIRSING, A E; LEE, L C
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 17
PI WO 9120095 A 19911226 (199203)*
RW: AT BE CH DE DK ES FR GB IT LU NL SE
W: BR CA JP
US 5130779 A 19920714 (199231) 15p H01L023-48
EP 540522 A1 19930512 (199319) EN 59p H01L023-485
R: BE CH DE DK ES FR GB IT LI NL SE
US 5251806 A 19931012 (199342) 16p H01L021-283
JP 05507174 W 19931014 (199346) 16p H01L021-321
CA 2084685 C 19960116 (199614) H01L023-485
AB WO 9120095 A UPAB: 19931006
A **solder** interconnection is claimed and comprises: a) a site for a **solder mass**, b) a **solder mass** formed on said site, and c) a material substantially encapsulating the **solder mass**.
More specifically, the side for the **solder mass** is on an active electronic component, partic. a chip, or a passive electronic component, partic. a substrate. USE/ADVANTAGE - Used for **solder** interconnections for electronic components at high mounting density in LSI circuits. Allows the reliability of controlled coallpse chip connection (c4) pads to be improved by providing a means to increase the chip to substrate height. @
4/17@
ABEQ US 5130779 A UPAB: 19931006
Solder interconnection (I) comprises (a) a site for a **solder mass**; (b) a first **solder mass** on site (a); and (c) a material encapsulating mass (b). Material (c) is an electrical conductor which is either (i) a **solder** wettable material selected from Co, Cu, Ni, Pd, Pt, Ru or alloys of these; or (ii) a non-**solder** wettable material selected from Be, Cr, Fe, Hf, Mo, Nb, Ta, Ti, V, W, Zr and alloys of these.
Pref., site (a) comprises a barrier material. Pref., (I) has an aspect ratio greater than 0.50.
ADVANTAGE - Scale up to chip size is enabled with integration of much more circuitry into a single chip.
4/17
ABEQ EP 540522 A UPAB: 19931113
A **solder** interconnection comprises; (a) a site for a **solder mass**, (b) a **solder mass** formed on the site, and (c) a material substantially encapsulating the **solder mass**.
More specifically, the side for the **solder mass** is on an active electronic component, partic. a chip or a passive electronic component partic. a substrate.
USE/ADVANTAGE - Used for **solder** interconnections for electronic components at high mounting density in LSI circuits. Allows the reliability of controlled coallpse chip connection pads to be improved by providing a means to increase the chip to substrate height.
ABEQ US 5251806 A UPAB: 19931202
Solder interconnection is formed by a method in which a **solder mass** (16) is formed and is encapsulated by a layer of electro conductive material (18), comprising a **solder** wettable material selected from the gp. Co, Cu, Ni, Pd, Rt, Ru or alloys of these, or a **solder** non-wettable material from the gp. Be, Cr, Fe, Hf, Mo, Nb, Ta, Ti, V, W, Zr or alloys of these. A 2nd **solder mass** (26) is formed in the 1st.

ADVANTAGE - No slumping, high structural integrity level.
Dwg.4/17

ABEQ JP 05507174 W UPAB: 19940103
A **solder** interconnection is claimed and comprises: (a) a site for a **solder mass**, (b) a **solder mass** formed on said site, and (c) a material substantially encapsulating the **solder mass**.

More specifically, the side for the **solder mass** is on an active electronic component, partic. a chip, or a passive electronic component, partic. a substrate.

USE/ADVANTAGE - Used for **solder** interconnections for electronic components at high mounting density in LSI circuits. Allows the reliability of controlled collapse chip connection (c4) pads to be improved by providing a means to increase the chip to substrate height.

FS CPI EPI
FA AB; GI
MC CPI: **L04-C17A**

L123 ANSWER 10 OF 10 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-132352 [16] WPIX
CR 1994-293619 [36]; 1997-525801 [48]; 1997-558042 [51]; 1999-069315 [06]; 1999-080544 [07]; 1999-560234 [47]; 2001-201283 [20]; 2002-237703 [29]; 2002-291248 [33]
DNN N1992-098714
TI Semiconductor chip assembly - has **flexible**, sheet-like elements with terminals which overlie surface of chip.
DC U11
IN DISTEFANO, T H; KHANDROS, I Y
PA (FIRS-N) 1ST ASSOC INC; (TESS-N) **TESSERA INC**; (ONES-N) 1ST ASSOC INC
CYC 21
PI WO 9205582 A 19920402 (199216)* EN 101p
RW: AT BE CH DE DK ES FR GB GR IT LU NL SE
W: AU CA FI JP KR SE SU US
AU 9187312 A 19920415 (199230) H01L023-12
US 5148265 A 19920915 (199240) 27p H01L023-12
US 5148266 A 19920915 (199240) 18p H01L023-12
EP 551382 A1 19930721 (199329) EN 2p H01L023-12
R: AT BE CH DE DK ES FR GB GR IT LI LU NL SE
US 5258330 A 19931102 (199345) 26p H01L021-60
JP 06504408 W 19940519 (199424) H01L021-60
US 5346861 A 19940913 (199436) 19p H01L021-60
EP 551382 A4 19930901 (199527)
US 5682061 A 19971028 (199749) 18p H01L023-48
KR 9705709 B1 19970419 (199939) H01L023-12
CA 2091438 C 20000808 (200051) EN H01L023-50
EP 1111672 A2 20010627 (200137) EN H01L021-822
R: AT BE CH DE DK ES FR GB GR IT LI LU NL SE
EP 551382 B1 20011219 (200206) EN H01L023-498
R: AT BE CH DE DK ES FR GB GR IT LI LU NL SE
DE 69132880 E 20020131 (200216) H01L023-498
ES 2167313 T3 20020516 (200239) H01L023-498
US 6392306 B1 20020521 (200241) H01L023-48
US 6465893 B1 20021015 (200276) H01L023-48
AB WO 9205582 A UPAB: 20021125
The semiconductor assembly includes a semiconductor chip having surfaces with contacts on at least one of the surfaces and a sheet (42) having terminals (48).

The sheet-like element and at least some of the terminals overlie the surface of the chip, The terminals are movable with respect to the chip and the assembly including a resilient layer for permitting movement of the terminals toward the chip.

ADVANTAGE - Improved method allowing compact assembly with compensation for **thermal expansion**.

Dwg.9/30
ABEQ US 5148265 A UPAB: 19931006
The semiconductor chip has contacts on the periphery of its top surface and an interposer overlying the central portion of the top surface. Peripheral contact leads extend inwardly from the peripheral contacts to central terminals on the interposer. The terminals on the interposer may be connected to a substrate using techniques commonly used in surface mounting of electrical devices, such as **solder** bonding. The leads and pref. the interposer, are **flexible** so that the terminals are movable w.r.t. the contacts on the chip, to compensate for **differential thermal expansion** of the chip and substrate. The terminals on the interposer may be disposed in an area array having terminals disposed at equal spacings throughout the area of the interposer, thus providing distances between the terminals while accommodating all of the terminals in an area approximately the same size as the area of the chip itself. The interposer may be provided with a **compliant** layer disposed between the terminals and the chip to permit slight vertical movement of the terminals towards the chip during testing operation.

The chip and interposer assembly may be electrically tested prior to assembly to the substrate. A **compliant** layer disposed between

the terminals and the chip permits slight vertical movement of the terminals towards the chip during testing operations in which the terminals on the interposer are engaged with an assembly of test probes.

ADVANTAGE - Entire assembly is compact.

3/16

ABEQ US 5148266 A UPAB: 19931006

The semiconductor chip assembly is mounted to contact pads in a compact area array. An interposer is disposed between the chip and the substrate. The contacts on the chip are connected to terminals on the interposer by **flexible** leads extending through apertures in the interposer. The terminals on the interposer in turn are bonded to the contact pads on the substrate.

Flexibility of the leads permits relative movement of the contacts on the chip relative to the terminals and the contact pads of the substrate and hence relieves the stresses caused by **differential thermal expansion**.

ADVANTAGE - Compact structure similar to that achieved through flip-chip bonding, but with markedly increased resistance to thermal cycling damage.

2/16

ABEQ EP 551382 A UPAB: 19931116

The semiconductor assembly includes a semiconductor chip having surfaces with contacts on at least one of the surfaces and a sheet (42) having terminals (48).

The sheet-like element and at least some of the terminals overlie the surface of the chip, The terminals are movable with respect to the chip and the assembly including a resilient layer for permitting movement of the terminals toward the chip.

ADVANTAGE - Improved method allowing compact assembly with compensation for **thermal expansion**.

Dwg.1/1

ABEQ US 5258330 A UPAB: 19931220

The semiconductor chip has contacts on the periphery of its top surface and has an intermediate dielectric layer overlying the central portion of the top surface. Peripheral contact leads extend inwardly from the peripheral contacts to central terminals on the dielectric sheet. The terminals on the dielectric may be connected to a substrate. The leads, and pref. the dielectric layer, are **flexible** so that the terminals are movable with respect to the contacts on the chip, to compensate for **differential thermal expansion** of the chip and substrate.

The terminals may be located in an area array with terminals positioned at equal spacings throughout the area of the dielectric, providing substantial distances between the terminals while accommodating all of the terminals in an area the same size as the chip area. The dielectric may have a **compliant** layer between the terminals and the chip to permit slight vertical movement of the terminals towards the chip during testing operations.

USE - E.g. RAM, muprocessor.

Dwg.3/16

ABEQ US 5346861 A UPAB: 19941102

The chip assembling method includes the steps of assembling a **flexible** sheetlike dielectric interposer formed separately from the chip and having first and second surfaces to the chip. A first surface of the interposer confronts a front surface of the chip, so that the first surface of the interposer bears on the front surface of the chip and a portion of the interposer overlies a contact pattern area encompassed by a pattern of contacts on the front surface of the chip.

The contacts on the chip are connected to terminals disposed on the second surface of the interposer within an area of the interposer overlying the contact pattern area by the **flexible** leads so that such leads extend between the contacts and terminals through apertures in the interposer and each such terminal is moveable with respect to the associated contact.

ADVANTAGE - Increased resistance to thermal cycling damage.

Dwg.2/16
ABEQ US 5682061 A UPAB: 19971211
A component for connecting a semiconductor chip to a substrate, said component being formed separately from the chip, said component comprising:
(a) a **flexible** sheetlike dielectric interposer having first and second surfaces and a plurality of apertures extending through the interposer from said first surface to said second surface;
(b) a plurality of terminals disposed on said second surface; and
(c) a **flexible**, electrically conductive lead extending from each said terminal to one of said apertures, each said lead having a contact end aligned with the associated aperture, said apertures and the contact ends of said leads being positioned in a pattern corresponding to a pattern of contacts on the chip, said interposer being **compliant** so that each terminal can be displaced in a direction perpendicular to the sheetlike interposer and a region of the interposer beneath each terminal can be compressed to accommodate such displacement.
Dwg.2,3/16
FS EPI

L101 ANSWER 4 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:710276 HCAPLUS
DN 128:6270
TI Tensile deformation behavior and thermal fatigue properties of Sn-Pb eutectic system solder alloys
AU Takemoto, Tadashi; Takahashi, Masahiro; Matsunawa, Akira; Yoshiura, Yozo
CS Joining Welding Res. Inst., Osaka Univ., Japan
SO Yosetsu Gakkai Ronbunshu (1997), 15(3), 541-546
CODEN: YGRODU; ISSN: 0288-4771
PB Yosetsu Gakkai
DT Journal
LA Japanese
CC 56-12 (Nonferrous Metals and Alloys)
AB Tensile deformation characteristics of Sn-Pb eutectic system solder alloys have been investigated using a strain rate changing tensile test to obtain strain rate sensitivity index in order to correlate the behavior to thermal fatigue properties. Mech. properties such as tensile stress and **elongation** were also obtained. These properties were compared for Sn-Sb eutectic and the Sn-Pb alloy contg. small amt. of Ag and Sb. The addn. of small amt. of Ag and Sb to Sn-Pb raised tensile strength and slightly decreased **elongation**. The alloys with these elements showed finer microstructure and higher resistance to thermal fatigue than plain eutectic. The soln. hardening and dispersion of Ag3Sn would be responsible to the enhanced tensile strength and resistance to thermal fatigue. Strain rate sensitivity index m was repeatedly obtained during tensile test. The plots between m and the strain where m was measured showed a straight relation, therefore, the extrapolated value of m to strain zero (m0), and the gradient of the line (k) were used as a parameter for the estn. of thermal fatigue resistance. The m0 decreased with the coarsening of microstructure due to aging at elevated temp., the value could be used as a measure of microstructural coarsening. The m0 and k might be a good measure to est. the thermal fatigue properties of solder alloys.
IT **37256-13-6**
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(tensile deformation behavior and thermal fatigue properties of Sn-Pb eutectic system **solder** alloys)
RN 37256-13-6 HCAPLUS
CN Tin alloy, base, Sn 63,Pb 37,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L13630) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	63	7440-31-5
Pb	37	7439-92-1
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

L101 ANSWER 5 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:431880 HCAPLUS
DN 127:84577
TI A study on mechanical properties of eutectic and solid solution Pb-Sn-Ag solders from -200.degree.c to 150.degree.c
AU Jones, W. K.; Liu, Y.; Zampino, M. A.; Gonzalez, G.; Shah, M.
CS Department of Mechanical Engineering, Florida International University, Miami, FL, 33199, USA
SO Design & Reliability of Solders and Solder Interconnections, Proceedings of a Symposium held during the TMS Annual Meeting, Orlando, Fla., Feb. 10-13, 1997 (1997), 85-96. Editor(s): Mahidhara, Rao K. Publisher: Minerals, Metals & Materials Society, Warrendale, Pa.
CODEN: 64QHAZ
DT Conference
LA English
CC 56-9 (Nonferrous Metals and Alloys)
AB The mech. properties of 5 Pb-Sn solders commonly used in electronic packaging were detd. from -200 to 150.degree. using a uniaxial tensile test, dynamic mech. anal. (DMA) and acoustic pulse methods. The following results were found: the elastic modulus decreases linearly with increasing temp. until 70.degree., and then rapidly drops >100.degree.; the strength of the eutectic solders (63Sn/37Pb, 62Sn/36Pb/2Ag, 96Sn/4Ag) decreases with increasing temp. while the strength remained fairly const. for the lead matrix solid soln. solders (5Sn/95Pb, and 10Sn/90Pb); the ductility change is complex: for the lead matrix solid soln. solders with increasing temp., the total **elongation** increases slowly, the uniform **elongation** is relatively high (>20%) and decreases slowly, and the neck **elongation** increases sharply. However, for the eutectic solders, super-plasticity occurs at temps. >100.degree., and brittle fracture occurs at temps. below -150.degree.. A peak of uniform **elongation** appears near the T/Tm = 0.5 for all the solders. Based on above studies, the deformation and fracture processes of the 5 solders were studied, and their fracture mechanism is proposed. A scanning electron microscope was used to examine the fracture and microstructure. For Pb-rich solid soln. solders (95Pb/5Sn and 90Pb/10Sn), which exhibit an FCC lead matrix, the linear relation of the mech. properties vs. the temp. is caused by ductile fracture mechanism which is uniform at -200-150.degree.. For Sn-rich matrix eutectic solders, 3 distinct stages of changes in **elongation** over the temp. range correspond to 3 different fracture mechanisms: superplastic fracture, ductile fracture and quasi-cleavage fracture.
RL: PRP (Properties)
(mech. properties of eutectic and solid soln. Pb-Sn-Ag **solders** from -200.degree. to 150.degree.)
RN 12641-81-5 HCAPLUS
CN Lead alloy, base, Pb 90,Sn 10 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	90	7439-92-1
Sn	10	7440-31-5

RN 37256-13-6 HCAPLUS
CN Tin alloy, base, Sn 63,Pb 37,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L13630) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	63	7440-31-5
Pb	37	7439-92-1
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6

Al	0	-	0.005	7429-90-5
Zn	0	-	0.005	7440-66-6

RN 39315-20-3 HCAPLUS
CN Lead alloy, base, Pb 95,Sn 5 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	95	7439-92-1
Sn	5	7440-31-5

RN 54341-62-7 HCAPLUS
CN Tin alloy, base, Sn 61.5-62.5,Pb 35-36,Ag 1.75-2.25,Sb 0-0.50,Bi 0-0.25,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005,Cd 0-0.001 (ASTM B32-Sn62) (9CI) (CA INDEX NAME)

Component	Component Percent			Component Registry Number
Sn	61.5	-	62.5	7440-31-5
Pb	35	-	37	7439-92-1
Ag	1.75	-	2.25	7440-22-4
Sb	0	-	0.50	7440-36-0
Bi	0	-	0.25	7440-69-9
Cu	0	-	0.08	7440-50-8
As	0	-	0.03	7440-38-2
Fe	0	-	0.02	7439-89-6
Al	0	-	0.005	7429-90-5
Zn	0	-	0.005	7440-66-6
Cd	0	-	0.001	7440-43-9

RN 68977-16-2 HCAPLUS
CN Tin alloy, base, Sn 96,Ag 3.6-4.4,Cu 0-0.20,Pb 0-0.10,As 0-0.05,Cd 0-0.005,Zn 0-0.005 (UNS L13961) (9CI) (CA INDEX NAME)

Component	Component Percent			Component Registry Number
Sn	96			7440-31-5
Ag	3.6	-	4.4	7440-22-4
Cu	0	-	0.20	7440-50-8
Pb	0	-	0.10	7439-92-1
As	0	-	0.05	7440-38-2
Cd	0	-	0.005	7440-43-9
Zn	0	-	0.005	7440-66-6

L124 ANSWER 25 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1993-167729 [20] WPIX
DNN N1993-128335 DNC C1993-074852
TI Lead-in metal substrate having resistance to loss **solderability** - comprising substrate coated with fusible **solder** coating contg. age resistant additive.
DC E14 L03 M23 P55 U11 V04
IN BISHOP, R L; EDGINGTON, R J; RIFE, R J
PA (NACO) NAT STANDARD CO
CYC 19
PI WO 9309276 A1 19930513 (199320)* EN 11p C25D003-32
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
W: AU CA JP KR
AU 9229273 A 19930607 (199338) C25D003-32
ADT WO 9309276 A1 WO 1992-US9134 19921028; AU 9229273 A AU 1992-29273 19921028
FDT AU 9229273 A Based on WO 9309276
PRAI US 1991-786594 19911101
REP US 3755096; US 3769182; US 3785929; US 3954573; US 4395294; US 4582576; US 4849059
IC ICM C25D003-32
ICS B23K035-36; C25D003-36; C25D003-60
AB WO 9309276 A UPAB: 19931113
A lead-in metal substrate possessing resistance to the loss of **solderabilty** due to ageing comprises a substrate coated with a fusible **solder** coating (I) contg. 0.5-20x10-4 wt% of an age resistant additive (II). Also claimed is a method of depositing a fusible **Sn/Pb solder** coating onto a cleaned lead-in metal substrate.

(II) is an aromatic aldehyde pref. benzaldehyde opt. substd. by nitro, amino, alkyl or halogen groups. (I) is obtained from a fluoborate or methylsulphonic and plating bath and has a coating thickness of 5-800 micro moles, contains 1.0-10x10power-4 wt. of (I) and has 90/10 wt% of **Sn/Pb**.

USE/ADVANTAGE - The **solder** coated metal substrate exhibits **long** term resistance to normal storage conditions and natural ageing thereby avoiding loss of **solderability**.

Dwg.0/0
FS CPI EPI GMPI

L124 ANSWER 27 OF 53 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-382820 [47] WPIX
DNN N1992-291852 DNC C1992-169869
TI **Solder** for mounting semiconductor chips - comprises tin -silver antimony alloy **solder** contg. aluminium to prevent oxide film formation on molten **solder**.
DC L03 M23 P55 U11 V04 X24
IN BARTH, M; ILLGEN, L; OSWALD, S; RATHMANN, R
PA (DEAK) AKAD WISSENSCHAFTEN DDR; (LEIS-N) LEISTUNGSELEKTRONIK STAHNSDORF AG; (DEAK) ZENT INST FESTKOERPERPHYSIK AKAD WISS
CYC 1
PI DD 300589 A7 19920625 (199247)* 3p B23K035-26
ADT DD 300589 A7 DD 1990-340938 19900523
PRAI DD 1990-340938 19900523
IC ICM B23K035-26
AB DD 300589 A UPAB: 19931006
A **solder**, for mounting semiconductor chips on conductive substrates, consists of a Sn-Ag-Sb alloy which contains 0.05-1.5 (pref. 0.05-0.2) wt.% Al.
ADVANTAGE - The **solder** produces **fatigue** resistant, **long** term stable joints with high tensile strength and good **thermal cycling** resistance, the aluminium addn. preventing formation of a wetting-inhibiting film on the molten **solder** in the presence of oxygen traces.
In an example a **solder** of compsn. (by wt.) 65% Sn, 24.9% Ag, 10% Sb and 0.10% Al was used in rapidly solidified strip form for automatic bonding of silicon chips to a copper carrier strip. **Soldering** was carried out at 240 deg.C for 5 sec. The **soldered** joints withstood 10000 cycles of 5 mins. heating by 65K and cooling without thermal **fatigue failure**.
0/0
FS CPI EPI GMPI
FA AB

L101 ANSWER 7 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:67590 HCAPLUS
DN 124:124239
TI Ultraplastic solder alloys
IN Nishihata, Mikio; Kunimine, Tatsuo; Asami, Kenji; Kubozono, Satoshi; Asami, Kuniaki
PA Nippon Beru Paatsu Kk, Japan; Nippon Handa Kk; Nippon Minichua Roopu Kk; Nippon Deeta Materiaru Kk
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT **Patent**
LA Japanese
IC ICM B23K035-26
ICS B23K035-40; C22C011-06; C22C013-00
ICI C22K003-00
CC 56-9 (Nonferrous Metals and Alloys)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07299584	A2	19951114	JP 1994-115968	19940502
PRAI	JP 1994-115968		19940502		

AB The alloys are Pb alloys contg. 40-70 wt.% Sn with **elongation** .gtoreq.1000% prepd. by melting (at max. 500.degree.) by reducing pressure (degree of vacuum 10-1-10-5 Torr). 3Rd elements such as Sb, Cu, Bi, Ag, P, and In may be added into the molten alloys to give the title alloys with **elongation** .gtoreq.500%. Foils and wires formed from the alloys are also claimed.
RL: PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(prepn. of ultraplastic **solder** lead-tin alloys)
RN 12641-87-1 HCAPLUS
CN Lead alloy, base, Pb 60,Sn 40,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.02,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L54915) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	60	7439-92-1
Sn	40	7440-31-5
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.02	7440-38-2
Fe	0 - 0.02	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

RN 37202-56-5 HCAPLUS
CN Lead alloy, base, Pb 50,Sn 50,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L55030) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	50	7439-92-1
Sn	50	7440-31-5
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

RN 37233-25-3 HCAPLUS
CN Tin alloy, base, Sn 70,Pb 30,Bi 0-0.25,Sb 0-0.20,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L13700) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	70	7440-31-5
Pb	30	7439-92-1
Bi	0 - 0.25	7440-69-9
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Sb	0 - 0.02	7440-36-0
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

RN 62258-61-1 HCAPLUS
CN Tin alloy, base, Sn 60,Pb 40,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.03,Fe 0-0.03,Al 0-0.005,Zn 0-0.005 (UNS L13600) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	60	7440-31-5
Pb	40	7439-92-1
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.03	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

RN 173079-99-7 HCAPLUS
CN Tin alloy, base, Sn 40-70,Pb 30-60 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	40 - 70	7440-31-5
Pb	30 - 60	7439-92-1

IT **54341-62-7 82061-99-2 172957-46-9**
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(prepn. of ultraplastic **solder** lead-tin alloys)
RN 54341-62-7 HCAPLUS
CN Tin alloy, base, Sn 61.5-62.5,Pb 35-36,Ag 1.75-2.25,Sb 0-0.50,Bi 0-0.25,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005,Cd 0-0.001 (ASTM B32-Sn62) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	61.5 - 62.5	7440-31-5
Pb	35 - 37	7439-92-1
Ag	1.75 - 2.25	7440-22-4
Sb	0 - 0.50	7440-36-0
Bi	0 - 0.25	7440-69-9
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6
Cd	0 - 0.001	7440-43-9

RN 82061-99-2 HCAPLUS
CN Tin alloy, base, Sn 63,Pb 37 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	63	7440-31-5
Pb	37	7439-92-1

RN 172957-46-9 HCAPLUS
CN Lead alloy, base, Pb 55,Sn 44,Sb 1,Cu 0.1 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	55	7439-92-1
Sn	44	7440-31-5
Sb	1	7440-36-0
Cu	0.1	7440-50-8

L121 ANSWER 7 OF 9 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1992-305979 [37] WPIX
DNN N1992-234119
TI Low stress tape-coat structure - has flex-coat applied between leads that have constant DC potential difference.
DC U11
PA (ANON) ANONYMOUS
CYC 1
PI RD 340089 A 19920810 (199237)* H01L000-00
ADT RD 340089 A RD 1992-340089 19920720
PRAI RD 1992-340089 19920720
IC ICM H01L000-00
AB RD 340089 A UPAB: 19931006
The coating thickens the flex, making it less **compliant** and does have adverse effects in **fatigue** properties, causing **fatigue** fracture much earlier in life than uncoated parts.

In the structure proposed, flexcoat is applied only between leads that have a constant DC potential difference (such as power and ground). Since most of the signal lines switch polarity regularly, dendrite formation between these lines will take much longer compared to that in a constant potential field. Thus, they need not be protected. On the other hand, the stiffness of the flex and the total force applied to the end leads is a linear function of the flexcoat volume. Therefore, the total stress will decrease in proportion to the uncoated areas on the flex. The stress redn. will be substantial if only one coats between power and ground leads. Alternately, one can coat every other line and protect the entire wiring from dendrite formation: total stiffening and stress will be significantly minimised. These structures can be mfd. by screening through a mask, or by blanket coating and selective laser ablation.

ADVANTAGE - Prevents electrolytes from getting between leads preventing dendrite formation.

FS EPI
FA AB
MC EPI: U11-D03A1B; **U11-D03B**

L124 ANSWER 53 OF 53 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1970:460481 HCAPLUS
DN 73:60481
TI Face-bonded semiconductor device utilizing **solder** surface tension balling effect
IN Ikeda, Koichi; Minagawa, Katsuji; Tanaka, Shigezo
PA Japan Electric Co., Ltd.
SO U.S., 5 pp.
CODEN: USXXAM
DT **Patent**
LA English
IC H01L
NCL 317234000
CC 71 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3517279	A	19700623	US 1967-668371	19670918
	GB 1151165	A	19690507	GB 1967-1151165	19670918
PRAI	JP 1966-61822		19660917		

AB A method is provided for forming protrusions on the bonding portions of a semiconductor element and/or a substrate to be face-bonded to each other. E.g., a planar transistor element having an n-type collector, a p-type base, and an n-type emitter is made of Si single crystal and one major surface is covered with a SiO2 film with windows open to a base and emitter. The element is typically 150-.mu. thick, and 600 .times. 400 .mu. in area. Al is evapd. over the SiO2 film and the 0.6-.mu. thick film is then photoetched to form electrode patterns. Each pattern includes a narrow region making contact with the emitter or base, another narrow region being **elongated** from the narrow contact region, and a circular broad region continuous to the narrow **elongated** region. Both the narrow and **elongated** regions are 10-.mu. wide, the diam. of the circular region being 70 .mu.. The distance between centers of the 2 broad regions is 150 .mu.. The emitter and base electrodes are completed by chem. plating Ni, 2-.mu. thick, and then Au, 0.2-.mu. thick, on the Al film. The element is dipped into fused In at 180.degree. for 10 sec to deposit In over the electrodes. The deposited In rises up to 5 .mu. max. height on the narrow regions of the emitter electrode or of the base electrode and also protrudes up to 35 .mu. max. height from the electrode surface on the broad region of the electrode. The **solder** protrusions formed are to be used in face-bonding. Over the bottom surface of the crystal another **solder** layer is provided. A 500-.ANG. thick film of Sn oxide is formed over the mirror polished surface of a borosilicate glass substrate 200-.mu. thick, 1-mm wide and 5-mm long. Ni is chem. plated over the oxide film. The oxide and Ni films are photoetched to leave terminal patterns. Each has a circular broad region, 70-.mu. diam., an **elongated** narrow region 10-.mu. wide and 225-.mu. long, and a claviform region of 500 .mu. max. width and 2.2 mm in length. The terminals are provided with a Au film 0.2-.mu. thick by chem. plating on the Ni film and dipped for 10 sec into a fused **solder** of **Sn** 62-**Pb** 38% alloy at 220.degree.. The **solder** is deposited over the terminal. Max. height on the circular portions, the narrow-region, and the claviform regions are 35 .mu., 5 .mu., and 200-250 .mu., resp. The transistor element is placed on the substrate so that the **solder** protrusions made **contact**. A reacting operation at 230.degree. for 5 sec is performed to fuse these **solder** protrusions. After cooling, the mixed **solder** bonds the element and substrate together. Each of the lead-out conductors of tape form is connected to the **solder** layer of the transistor element and to the **solder** protrusions formed on the claviform regions of the substrate terminal. A face-bonded transistor device is completed by molding the face-bonded assembly with an epoxy resin.

L101 ANSWER 10 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1992:226053 HCAPLUS
DN 116:226053
TI Constant strain rate tensile properties of various lead based solder alloys at 0, 50, and 100.degree.C
AU Cole, M. S.; Caulfield, T.; Banks, D. R.; Winton, M. M.; Walsh, A. P.; Gonya, S. G.
CS Gen. Technol. Div., IBM Corp., Hopewell Junction, NY, USA
SO Mater. Dev. Microelectron. Packag.: Perform. Reliab., Proc. Electron. Mater. Process. Congr., 4th (1991), 241-9. Editor(s): Singh, Prabjit. Publisher: ASM Int., Materials Park, Ohio.
CODEN: 57QLAN
DT Conference
LA English
CC 76-14 (Electric Phenomena)
Section cross-reference(s): 56
AB The tensile properties were detd. at 0, 50, and 100.degree. and at 10-6/s strain rate of various high and low m.p. solders. The low m.p. alloys are eutectic Sn-Pb, 2% Ag and 1.5% Sb addns. to eutectic Sn-Pb, and 70/30 Sn-Pb. The high m.p. alloys are 90/10 Pb-Sn, 97/3 Pb-Sn, and 95/5 Pb-In. Temp. and alloy trends for Young's modulus, yield strength, ultimate tensile strength, and **elongation** are discussed. These property trends are correlated to fracture surface and microstructural characteristics.
IT **12610-69-4 12641-81-5 37233-25-3 37256-13-6**
RL: USES (Uses)
(mech. properties of interconnection **solder** of)
RN 12610-69-4 HCAPLUS
CN Lead alloy, base, Pb 97,Sn 3 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	97	7439-92-1
Sn	3	7440-31-5

RN 12641-81-5 HCAPLUS
CN Lead alloy, base, Pb 90,Sn 10 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	90	7439-92-1
Sn	10	7440-31-5

RN 37233-25-3 HCAPLUS
CN Tin alloy, base, Sn 70,Pb 30,Bi 0-0.25,Sb 0-0.20,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L13700) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	70	7440-31-5
Pb	30	7439-92-1
Bi	0 - 0.25	7440-69-9
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Sb	0 - 0.02	7440-36-0
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

RN 37256-13-6 HCAPLUS
CN Tin alloy, base, Sn 63,Pb 37,Bi 0-0.25,Sb 0-0.12,Cu 0-0.08,As 0-0.03,Fe 0-0.02,Al 0-0.005,Zn 0-0.005 (UNS L13630) (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Sn	63	7440-31-5
Pb	37	7439-92-1
Bi	0 - 0.25	7440-69-9
Sb	0 - 0.12	7440-36-0
Cu	0 - 0.08	7440-50-8
As	0 - 0.03	7440-38-2
Fe	0 - 0.02	7439-89-6
Al	0 - 0.005	7429-90-5
Zn	0 - 0.005	7440-66-6

L101 ANSWER 13 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1990:203200 HCAPLUS
DN 112:203200
TI Diffusion processes and their modifications in some lead-tin-copper alloy solders
AU Gupta, D.; Oberschmidt, J.
CS T. J. Watson Res. Cent., IBM, Yorktown Heights, NY, 10598, USA
SO Diffusion and Defect Data--Solid State Data, Pt. A: Defect and Diffusion Forum (1990), 66-69(Diffus. Met. Alloys-DIMETA 88, Pt. 2), 605-23
CODEN: DDAFE7; ISSN: 1012-0386
DT Journal
LA English
CC 56-12 (Nonferrous Metals and Alloys)
AB Lattice and grain boundary radioactive tracer diffusion measurements were made in Pb-Sn and Pb-Sn-Cu alloy solders commonly employed in very large scale integrated circuit **interconnections**. The nominal Sn content in all cases was 8 at.%, while the Cu content was 0, 1.4, 4.3, and 10.5 at.%. The diffusion coeffs. in the ternary alloys are compared with those in pure Pb and the Pb-8.3 at.% Sn binary alloy. Increasing addns. of Cu to the Pb-Sn binary alloy reduces the grain boundary diffusion of Pb. The lattice diffusivity of Pb decreases only when the Cu content reaches 10.5 at.%. The results in the ternary alloys having lower Cu content are comparable to those in the binary Pb-Sn alloy. The microstructure and energy dispersive x-ray anal. results show that the Cu-Sn intermetallic compd. formation exts. Cu and Sn atoms from the lattice. The attendant increase in the m.p. of the matrix thereby lowers the diffusion. The redn. in the grain-boundary diffusion is due to the pptn. of the Cu-Sn intermetallic compd. into the grain-boundaries by a mechanism in which free vol. and mobile defects are eliminated. From the measured diffusion coeffs. of the 2 kinds, the solute segregation factors were computed in the various alloys as function of temp. The extent of grain-boundary segregation and its thermal stability in the ternary alloy substantiate the mechanism.
IT **126897-42-5**, Copper 0.3, lead 95, tin 5 **126897-43-6**
126897-44-7, Copper 3.5, lead 92, tin 5
RL: USES (Uses)
(diffusion of lead and tin in **solder** of)
RN 126897-42-5 HCAPLUS
CN Lead alloy, base, Pb 95,Sn 5,Cu 0.3 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	95	7439-92-1
Sn	5	7440-31-5
Cu	0.3	7440-50-8

RN 126897-43-6 HCAPLUS
CN Lead alloy, base, Pb 94,Sn 5,Cu 1.4 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	94	7439-92-1
Sn	5	7440-31-5
Cu	1.4	7440-50-8

RN 126897-44-7 HCAPLUS
CN Lead alloy, base, Pb 92,Sn 5,Cu 3.5 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	92	7439-92-1
Sn	5	7440-31-5
Cu	3.5	7440-50-8

L101 ANSWER 15 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1987:218013 HCAPLUS
DN 106:218013
TI The effect of copper-tin (Cu6Sn5) whisker precipitates in bulk 60Sn-40Pb solder
AU Frear, Darrel; Grivas, Dennis; Morris, J. W., Jr.
CS Cent. Adv. Mater., Lawrence Berkeley Lab., Berkeley, CA, 94720, USA
SO Journal of Electronic Materials (1987), 16(3), 181-6
CODEN: JECMA5; ISSN: 0361-5235
DT Journal
LA English
CC 56-9 (Nonferrous Metals and Alloys)
AB Hollow Cu6Sn5 [12019-69-1] intermetallic compd. rods form within molten 60Sn-40Pb [62258-61-1] **solder** when it reacts with Cu. These rods form at the Cu surface by a screw dislocation mechanism and break off into the bulk **solder**. Hollow hexagonal intermetallics result when the core of the rod dissolves away and fills with molten **solder**. The mech. properties of bulk 60Sn-40Pb **solder** with and without the Cu6Sn5 intermetallic rods were detd. in tension at -196 to 125.degree.. The intermetallics had no effect on strength, but decreased **elongation** at the lower temps. The intermetallics had a large effect on the fracture characteristics. At -196.degree., failure initiates by interfacial sepn. between the intermetallic and **solder** matrix. At 20.degree., failure initiates at cleaved intermetallic rods. At 125.degree., the intermetallic rods have little effect on the mech. properties.

L101 ANSWER 16 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1987:77291 HCAPLUS
DN 106:77291
TI Lead base alloys and their application for reducing electromigration activity
IN Fouts, David Perry; Gupta, Devandra; Ho, Paul Siu Chung; Jaspal, Jasvir Singh; Lloyd, James Robert, Jr.; Oberschmidt, James Michael; Skikrishnan, Kris Venkatraman; Sullivan, Michael James
PA International Business Machines Corp., USA
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT **Patent**
LA English
IC ICM B23K035-26
ICS C22C011-06
CC 76-13 (Electric Phenomena)
Section cross-reference(s): 56
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 198353	A2	19861022	EP 1986-104600	19860404
	EP 198353	A3	19880914		
	EP 198353	B1	19960724		
	R: DE, FR, GB, IT				
	US 4622205	A	19861111	US 1985-722631	19850412
	CA 1257786	A1	19890725	CA 1985-498313	19851220
	JP 61238932	A2	19861024	JP 1986-29158	19860214
	JP 03027317	B4	19910415		
PRAI	US 1985-722631		19850412		

AB The solder compn. consists essentially of a Pb-base alloy including a substantially uniform distribution of .gtoreq.1 intermetallic compd. e.g. Cu3Sn formed from the alloy and a solute element, the concn. of the solute element being .gtorsim. 0.5 wt. % of the amt. of the alloy. The compn. is applied for reducing electromigration activity and extending the lifetime of **terminations** in microelectronic devices.
IT **106555-07-1**
RL: USES (Uses)
(**solder** compn. contg., for reducing micromigration activity in microelectronic device **terminations**)
RN 106555-07-1 HCAPLUS
CN Lead alloy, base, Pb 92,Sn 4.8,Cu 3.4 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	92	7439-92-1
Sn	4.8	7440-31-5
Cu	3.4	7440-50-8

L101 ANSWER 19 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1986:54964 HCAPLUS
DN 104:54964
TI Fatigue-resistant solders
IN Asami, Kenji; Kageyama, Nobuo
PA Nippon Handa Kogyo K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT **Patent**
LA Japanese
IC ICM B23K035-26
ICS C22C011-06
CC 56-3 (Nonferrous Metals and Alloys)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 60166191	A2	19850829	JP 1984-19654	19840206
	JP 01024599	B4	19890512		
PRAI	JP 1984-19654		19840206		

AB A fatigue-resistant solder consists of Sn 20-47, Bi 2-12, Cu 0.03-0.5%, and Pb balance. The solder is used for electronic circuits. Thus, a solder consisting of Bi 8, Cu 0.05, Sn 46%, and Pb balance had 4.0 kg/mm2 tensile strength and 425% **elongation** as compared to 3.2 kg/mm2 and 80%, resp. for Sn 40-Pb 60 solder. The solder strength was av. 1110 g as compared to 360 g for Sn-15 Bi-40% Pb solder.

IT **100110-21-2**
RL: USES (Uses)
(**solder**,)
RN 100110-21-2 HCAPLUS
CN Lead alloy, base, Pb 46,Sn 46,Bi 8,Cu 0.2-0.4 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	46	7439-92-1
Sn	46	7440-31-5
Bi	8	7440-69-9
Cu	0.2 - 0.4	7440-50-8

L101 ANSWER 21 OF 27 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1985:117935 HCAPLUS
DN 102:117935
TI Structures and tensile properties of cast solder lead-tin alloys
AU Satoh, Ryohei; Ohshima, Muneo; Arakawa, Katsuhiro; Hirota, Kazuo
CS Prod. Eng. Res. Lab., Hitachi Ltd., Yokohama, Japan
SO Nippon Kinzoku Gakkaishi (1985), 49(1), 26-33
CODEN: NIKGAV; ISSN: 0369-4186
DT Journal
LA Japanese
CC 56-9 (Nonferrous Metals and Alloys)
Section cross-reference(s): 76
AB An investigation was made of the structure and tensile properties of the Pb-Sn solders which are important microsoldering and bonding materials used in the fabrication of semiconductors ICs(Integrated Circuit) and LSIs(Large Scale Integrated circuit). During the soldering operation the Pb-Sn alloys undergo a melting and solidifying process, and are in the so-called cast state; they exhibit a structure with significant segregation in the compn. This structure is thought to have a large influence on the reliability of the soldered joint. To evaluate the mech. properties of the microsoldered joint, cast solders (Pb/Sn 100, 99/1, 97/3, 95/5, 93/7, 90/10, 85/15 and 37/63 (eutectic compn.)) were solidified and formed at the conventional cooling rate (.apprx.1 K/s). The microstructure and tensile properties were investigated. The cast solders exhibited a dendrite structure with the segregation of compn. They show very little **elongation** as compared with rolled materials. For Pb-rich solder alloys, tensile deformation occurred primarily within the grains, and virtually no grain boundary sliding of the type seen in rolled materials was obsd. Eutectic phase crystals, caused by the concns. of Sn in the grain boundary and between the dendrites (i.e., within the grains), were obsd. in the cast structure as a result of segregation in compn. In Pb-rich solders, this eutectic phase suppressed the rotation of the grains and grain boundary sliding, and thereby caused the redn. of tensile **elongation**.
IT **95393-03-6**
RL: USES (Uses)
(cast **solders** of, mech. properties and structure of)
RN 95393-03-6 HCAPLUS
CN Lead alloy, base, Pb 37-100,Sn 0-63 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Pb	37 - 100	7439-92-1
Sn	0 - 63	7440-31-5

L109 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1979:544587 HCAPLUS
DN 91:144587
TI Coefficient of linear **thermal expansion** of the alloys of **lead-tin**, bismuth-tin, and bismuth-cadmium systems and applicability of addition lows
AU Mavrodiev, G.; Koneska, S.
CS Fac. Phys., Skopje, Yugoslavia
SO Prilozi - Makedonska Akademija na Naukite i Umetnostite, Oddelenie za Prirodo-Matematicki Nauki (1976), 8(1), 19-27
CODEN: PMANDL; ISSN: 0581-0833
DT Journal
LA English
CC 56-7 (Nonferrous Metals and Alloys)
AB The **thermal expansion** coeffs. of solid **Pb-Sn** [12658-34-3], Bi-Sn [11134-03-5], and Bi-Cd [37239-64-8] system alloys were investigated. The obsd. behavior was probably due to microstresses set up between the individual phases as a result of **differential thermal expansion**. In the vicinity of the eutectic compn., the results were better fitted by the J. P. Thomas relation than by the rule of mixts.

L109 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1960:1407 HCAPLUS
DN 54:1407
OREF 54:217f-h
TI Mechanical and physical properties of three low-shrinkage **copper** -base casting alloys
AU Kura, J. G.; Lang, R. M.
CS Battelle Mem. Inst., Columbus, O.
SO Am. Soc. Testing Materials Proc. (1959), Volume Date 1958, 58, 775-90
DT Journal
LA Unavailable
CC 9 (Metallurgy)
AB cf. following abstr. Data were obtained on 16 mech. and phys. properties of 80-10-10, 85-5-5-5, and Navy "M" (88-6-1.5-4.5) alloys (**Cu**-**Sn**-**Pb**-Zn, resp.) at temps. ranging from -40 to 550.degree.F. Properties investigated included ultimate strength, yield strength, **elongation**, reduction of area, Young's modulus, compressive strength, V-notch Charpy impact strength, Brinell hardness, fatigue, machinability, melting range, patternmaker's shrinkage, d. and sp. gr., elec. resistivity, thermal cond., and **thermal expansion**.

11/9/9
DIALOG(R)File 2:INSPEC

5900430 INSPEC Abstract Number: B9806-0170J-011
Title: Flip chip **solder interconnections** : a reliability perspective
Author(s): Puttlitz, K.J.; Quinones, H.
Author Affiliation: IBM Microelectron., Hopewell Junction, NY, USA
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting p.359-66
Editor(s): Mahidhara, R.K.; Frear, D.R.; Sastry, S.M.L.; Murty, K.L.; Liaw, P.K.; Winterbottom, W.L.
Publisher: TMS, Warrendale, PA, USA
Publication Date: 1997 Country of Publication: USA xi+448 pp.
ISBN: 0 87339 354 6 Material Identity Number: XX98-00492
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting
Conference Sponsor: TMS
Conference Date: 10-13 Feb. 1997 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: The **solder** ball flip chip or so called C-4 connection was introduced by IBM nearly three decades ago as an alternative to manual wire bonding, whose productivity and reliability were not acceptable at that time. A very large field database indicates that flip-chip **interconnections** have been the most reliable die **interconnection** scheme in the industry since their inception. The technology is **flexible** , having been utilized with various types of chip carrier. Several unique technology features such as chip-level hermiticity and modifications made to enhance reliability as the technology evolved are discussed. The potential loss of integrity of flip-chip **solder** joints due to fatigue failure is an issue that has received considerable attention. Fatigue failure can result if thermally-induced strains within a joint generated by the mismatch in coefficient of **thermal expansion** (**CTE**) between die and chip carrier become too great. The influence of design and material parameters to reduce strain and dissipate stress are thus also discussed. The so-called modified Coffin-Manson (C-M) relationship provides the capability of predicting field life times based on standard laboratory tests. The basis of the C-M relationship is described and also modifications made to address creep, a common occurrence in **solder** applications. Flip-chip **solder** joint technology is sufficiently extendible to satisfy anticipated future I/O requirements. To meet these requirements the reliability impact of chip underfill, a recent development, is also discussed. (37 Refs)
Subfile: B
Descriptors: creep; encapsulation; fatigue; flip-chip devices; integrated circuit packaging; integrated circuit reliability; microassembling; **thermal expansion**; thermal stresses

4/9/8
DIALOG(R)File 2:INSPEC

5894533 INSPEC Abstract Number: B9805-0170J-061
Title: Diffusion processes in lead based **solders** used in microelectronic industry
Author(s): Gupta, D.; Oberschmidt, J.M.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting p.59-64
Editor(s): Mahidhara, R.K.; Frear, D.R.; Sastry, S.M.L.; Murty, K.L.; Liaw, P.K.; Winterbottom, W.L.
Publisher: TMS, Warrendale, PA, USA
Publication Date: 1997 Country of Publication: USA xi+448 pp.
ISBN: 0 87339 354 6 Material Identity Number: XX98-00492
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting
Conference Sponsor: TMS
Conference Date: 10-13 Feb. 1997 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: We have compiled parameters for /sup 203/Pb and /sup 119/Sn radiotracer diffusion in Pb, PbSn binary, PbSnCu, and PbSnAu ternary **solder** alloys in the lattice and in the grain boundaries. These isotopes represent the major elements of the **solders** . At a temperature of 80 degrees C, which is commonly observed during the use of **solders** in microelectronic applications, diffusion in both the lattice and grain boundaries have been found to be sizable, so that effective diffusion coefficients must be used for estimation of reliability due to processes such as cyclic creep, electromigration, thermomigration, etc. Significant reduction in the effective diffusion coefficients have been observed upon additions of ternary solutes such as Cu and Au. (12 Refs)
Chemical Indexing:
Pb int - Pb el (Elements - 1)
PbSn int - Pb int - Sn int - PbSn bin - Pb bin - Sn bin (Elements - 2)
PbSnCu int - Cu int - Pb int - Sn int - PbSnCu ss - **Cu ss - Pb ss - Sn ss** (Elements - 3)
PbSnAu int - Au int - Pb int - Sn int - PbSnAu ss - Au ss - Pb ss - Sn ss (Elements - 3)
Numerical Indexing: temperature 3.53E+02 K

4/9/9
DIALOG(R)File 2:INSPEC

5673400 INSPEC Abstract Number: B9710-0530-002
Title: Hard-particle reinforced composite **solders** . 1. Microcharacterisation
Author(s): Marshall, J.L.; Calderon, J.
Author Affiliation: Dept. of Chem., North Texas Univ., Denton, TX, USA
Journal: Soldering & Surface Mount Technology vol.9, no.2 p.22-8
Publisher: MCB University Press,
Publication Date: July 1997 Country of Publication: UK
CODEN: SSMOEO ISSN: 0954-0911
SICI: 0954-0911(199707)9:2L.22:HPRC;1-I
Material Identity Number: B310-97002
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: A series of composite **solders** in 63/37 Sn/Pb was prepared: Cu/sub 6/Sn/sub 5/ (10, 20, 30 wt%); Cu/sub 3/Sn (10, 20, 30 wt%); Cu (7.6 wt%); Ag (4 wt%); and Ni (4 wt%). These composite **solders** were prepared by two procedures: (A) admixture with **solder** paste; and (B) admixture with molten **solder** . The original particulates and the final composite **solders** were analysed and characterised by SEM (scanning electron microscopy), EDX (energy dispersive X-ray), and ESCA (electron spectroscopy for chemical analysis); or XPS (X-ray photoelectron spectroscopy). A variety of morphological characterisations, intermetallics and porosities were noted. Good wetting was noted in all cases, and porosity was greater for method (A). The particulates all exhibited excellent binding to the **solder** matrix. (21 Refs)
Chemical Indexing:
SnPbCu6Sn5 ss - Cu6 ss - Sn5 ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)
SnPbCu3Sn ss - Cu3 ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)
SnPbCu ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)
SnPbAg ss - Ag ss - Pb ss - Sn ss (Elements - 3)
SnPbNi ss - Ni ss - Pb ss - Sn ss (Elements - 3)

7/9/4
DIALOG(R)File 2:INSPEC

5456737 INSPEC Abstract Number: B9702-0170J-034
Title: Global" and "local" thermal mismatch stresses in an **elongated** bi-material assembly adhesively bonded at the ends
Author(s): Suhir, E.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Conference Title: Structural Analysis in Microelectronic and Fiber Optic Systems. 1995 ASME International Mechanical Engineering Congress and Exposition (EEP-Vol.12) p.101-5
Editor(s): Suhir, E.
Publisher: ASME, New York, NY, USA
Publication Date: 1995 Country of Publication: USA v+195 pp.
ISBN: 0 7918 1737 7 Material Identity Number: XX96-02958
Conference Title: Structural Analysis in Microelectronic and Fiber Optic Systems. 1995 ASME International Mechanical Engineering Congress and Exposition (EEP-Vol.12)
Conference Sponsor: ASME
Conference Date: 12-17 Nov. 1995 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: A simple stress model, based on a strength-of-materials approach, is developed for the evaluation of thermally induced stresses in an **elongated** bi-material assembly bonded at the ends and subjected to changes in temperature. The emphasis is on the interaction of the "global" thermal mismatch, counted with respect to the midcross-section of the assembly as a whole, and the "local" mismatch which is counted with respect to the midcross-sections of the bonded regions. The developed model is a generalization of a theory developed earlier for the case of a continuous bond (Suhir, ASME J. Appl. Mech., vol. 53, no. 3, 1986). (1 Refs)
Subfile: B
Descriptors: adhesion; bimetals; flip-chip devices; integrated circuit interconnections; packaging; **soldering**; stress analysis; **thermal expansion**; thermal stresses

11/9/11
DIALOG(R)File 2:INSPEC

5342665 INSPEC Abstract Number: B9609-0170J-071
Title: Fluxless flip-chip bonding on **flexible** substrates: A comparison between adhesive bonding and **soldering**
Author(s): Aschenbrenner, R.; Zakel, E.; Azdasht, G.; Kloeser, A.; Reichl, H.
Author Affiliation: Fraunhofer-Inst. fur Zuverlassigkeit und Mikrointegration, Berlin, Germany
Journal: Soldering & Surface Mount Technology no.23 p.5-11
Publisher: Wela Publications,
Publication Date: June 1996 Country of Publication: UK
CODEN: SSMOEO ISSN: 0954-0911
SICI: 0954-0911(199606)23L.5:FFCB;1-L
Material Identity Number: B310-96002
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: During the last few years, an increasing number of flip-chip (FC) **interconnection** technologies have emerged. While flip-chip assembly offers many advantages compared with conventional packaging techniques, several aspects prevent this technology from entering the high volume market. Among these are the availability of bumped chips and the costs of the substrates, i.e. ceramic substrates with closely matching coefficient of **thermal expansion** (**CTE**) to the chip, in order to maintain high reliability. Only recently, with the possibility of filling the gap between chip and organic substrate with an encapsulant, was the reliability of flip-chips mounted on organic substrates significantly enhanced. This paper presents two approaches to a fluxless process, one based on **soldering** techniques using Au-Sn metallurgy and the other on adhesive joining techniques. **Soldering** is performed with a thermode and with a laser based system. For both of these FC-joining processes, alternative bump metallurgies based on electroplated gold, electroplated gold-tin, mechanical gold and electroless nickel gold bumps are applied. (37 Refs)

11/9/12
DIALOG(R)File 2:INSPEC

5237796 INSPEC Abstract Number: B9605-0170J-159
Title: Material science and the electronic packaging roadmap
Author(s): Steidel, C.A.; Sundahl, R.C.; Grayeli, N.
Conference Title: Electronic Packaging Materials Science VIII. Symposium p.3-8
Editor(s): Sundahl, R.C.; Tu, K.-T.; Jackson, K.A.; Borgesen, P.
Publisher: Mater Res. Soc, Pittsburgh, PA, USA
Publication Date: 1995 Country of Publication: USA xi+284 pp.
Material Identity Number: XX96-00317
Conference Title: Electronic Packaging Materials Science VIII. Symposium
Conference Date: 17-20 April 1995 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: High performance/low cost packaging solutions for future products require sound understanding of the relations between material properties and package performance, manufacturability, reliability and quality. Both end point properties and in-process properties must be understood and characterized. These relationships are currently poorly defined, and the metrology tools needed to establish and confirm these relationships have not been rigorously applied. We thus experience long development cycles, high development cost and processes with narrow manufacturing windows. This paper discusses a case study on flip chip technology. The technical challenges for this integrated system include: **CTE** mismatch between chip and board; **interconnect** metallurgy for flip chip bump; flip chip design, including **flexibility** for use as a wirebond device; thermal management in a dense system; board pad size to receive flip chips; board wireability; known good die; timely availability of all the enabling technologies at reasonable cost. The complexity of the number of capabilities that must be brought together is an impediment to rapid technology deployment. All capabilities must first be planned and integrated for successful implementation. To illustrate potential challenges for the material developer, we look at two of the challenges noted above - **CTE** mismatch management and chip **interconnect** and design **flexibility**. (4 Refs)
Subfile: B
Descriptors: circuit reliability; cooling; flip-chip devices; integrated circuit **interconnections**; integrated circuit packaging; lead bonding; printed circuit design; printed circuit manufacture; printed circuit testing; quality control; **soldering**; test equipment; **thermal expansion**

4/9/10
DIALOG(R)File 2:INSPEC

5195901 INSPEC Abstract Number: A9607-8140N-009
Title: Creep-fatigue life prediction of in situ composite **solders**
Author(s): Kuo, C.G.; Sastry, S.M.L.; Jerina, K.L.
Author Affiliation: Washington Univ., St. Louis, MO, USA
Journal: Metallurgical and Materials Transactions A (Physical Metallurgy and Materials Science) Conference Title: Metall. Mater. Trans. A, Phys. Metall. Mater. Sci. (USA) vol.26A, no.12 p.3265-75
Publisher: Minerals, Metals & Mater. Soc. & ASM Int,
Publication Date: Dec. 1995 Country of Publication: USA
CODEN: MTTABN ISSN: 1073-5623
SICI: 1073-5623(199512)26A:12L.3265:CFLP;1-F
Material Identity Number: C077-96001
U.S. Copyright Clearance Center Code: 1073-5623/95/$00.75
Conference Title: Creep and Fatigue of Metal Matrix Composites
Conference Date: 1994 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Eutectic tin-lead **solder** alloys subjected to cyclic loading at room temperature experience creep-fatigue interactions due to high homologous temperature. Intermetallic reinforcements of Ni/sub 3/Sn/sub 4/ and Cu/sub 6/Sn/sub 5/ are incorporated into eutectic tin lead alloy by rapid solidification processes to form in situ composite **solders**. In this study, the in situ composite **solders** were subjected to combined creep and fatigue deformation at room temperature. Under cyclic deformation, the dominant damage mechanism of in situ composite **solders** is proposed to be growth of cavities. A constrained cavity growth model is applied to predict creep-fatigue life by taking into account the tensile loading component, as well as the compressive loading component when reversed processes can occur. An algorithm to calculate cavity growth in each fatigue cycle is used to predict the number of fatigue cycles to failure, based on a critical cavity size of failure. Calculated lives are compared to experimental data under several fatigue histories, which include. fully reversed stress-controlled fatigue, zero-tension stress-controlled fatigue, stress-controlled fatigue with tension hold time, fully reversed strain-controlled fatigue, and zero-tension strain-controlled fatigue. The model predicts the creep-fatigue lives within a factor of 2, with the incorporation of an appropriate compressive healing factor in most cases. Discrepancy between calculated lives and experimental results is discussed. (32 Refs)
Subfile: A
Chemical Indexing:
Ni3Sn4SnPb ss - Ni3 ss - Sn4 ss - Ni ss - Pb ss - Sn ss (Elements - 3)
Cu6Sn5SnPb ss - Cu6 ss - Sn5 ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)

4/9/11
DIALOG(R)File 2:INSPEC

5170964 INSPEC Abstract Number: B9603-2210D-019
Title: Alternatives to hot air **solder** leveling [Fine pitch SMT]
Author(s): Langan, J.P.
Conference Title: Proceedings of the Technical Program. NEPCON WEST `95 Part vol.2 p.691-6 vol.2
Publisher: Reed Exhibition Companies, Norwalk, CT, USA
Publication Date: 1995 Country of Publication: USA 3 vol. 1994 pp.
Material Identity Number: XX95-03008
Conference Title: Proceedings NEPCON West 95
Conference Date: 26 Feb.-2 March 1995 Conference Location: Anaheim, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: During the last 10 years, hot air **solder** leveled coatings (HASL) have replaced reflowed tin/lead electrodeposits as the preferred coating for preserving **solderability**. However, as packaging density increased, HASL`s shortcomings were discovered. When a copper pad or trace is hot coated or electroplated and fused, the tin/lead coating forms a meniscus, and the centre of the pad or trace is much thicker than the edges. Fine pitch SMDs need a flatter and more uniform coating thickness. To achieve this, the thickness must be reduced to lessen the meniscus height in the pad centre. Some pads may then be too thin and thus lead to **solderability** problems. With narrow leads inherent to fine pitch components, the amount of **solder** in a fillet is also crucial. The fillet is composed of tin/lead from the pad, the lead and the **solder** paste. The volume of **solder** paste and component plating thickness can be controlled but **solder** leveling presents a dilemma. This paper discusses alternatives to HASL for preserving **solderability** , including fused **solder** paste, flat fused **solder**, electroless tin/lead, electroless gold over nickel, preflux, inhibitor coatings, and combination inhibitor/preflux. (2 Refs)
Subfile: B
Chemical Indexing:
SnPbCu sur - Cu sur - Pb sur - Sn sur - SnPbCu ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)
Cu sur - Cu el (Elements - 1)
Au-Ni int - Au int - Ni int - Au el - Ni el (Elements - 1,1,2)
Ni sur - Ni el (Elements - 1)
Numerical Indexing: time 3.2E+08 s

11/9/13
DIALOG(R)File 2:INSPEC

5099096 INSPEC Abstract Number: B9512-0170J-057
Title: Assembly and reliability of very large flip-chip on CQFP
Author(s): Clementi, J.J.; Dearing, G.O.; Bergeron, C.
Author Affiliation: Div. of Microelectron., IBM Corp., Endicott, NY, USA
Conference Title: Proceedings of the 1994 International Electronics Packaging Conference p.296-307
Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA
Publication Date: 1994 Country of Publication: USA 916 pp.
Conference Title: Proceedings of International Electronics Packaging Conference
Conference Sponsor: Int. Electron. Packaging Soc
Conference Date: 25-28 Sept. 1994 Conference Location: Atlanta, GA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: The IBM ceramic quad flat pack (CQFP) is a high performance, low cost chip carrier for surface mount assembly. These finished modules conform to JEDEC I/O and footprint standards. They are available in 0.5 mm and 0.4 mm lead pitches with **flexibility** to address unique application requirements. Connection from IC to carrier is performed using flip-chip C4 (controlled collapse chip connection) attach. Silicon die size and quantity of C4 connections for flip-chip joining has historically been constrained to reduce early life failures caused by **solder** fatigue wearout. This DNP (distance from neutral point of chip footprint) limitation has been overcome with increasing usage of epoxy encapsulation as flip-chip underfill. The encapsulant matches the coefficient of **thermal expansion** (**CTE**) of C4 **solder** and minimizes stresses on the **interconnection** . This enhancement provides substantial reliability improvement in comparison to unencapsulated packages. Also, it enables larger die with smaller C4 **solder** bumps on finer pitches to be assembled on ceramic carriers. Recent product development and testing have extended flip-chip on ceramic packaging technology even further than previously anticipated. Test die up to 20 mm in size with over 2000 C4 joints have been successfully assembled, encapsulated, stress tested and qualified in CQFP modules. (12 Refs)
Subfile: B
Descriptors: assembling; ceramics; encapsulation; failure analysis; flip-chip devices; integrated circuit **interconnections**; integrated circuit manufacture; integrated circuit packaging; integrated circuit reliability; modules; polymers; **soldering**; standards; surface mount technology; **thermal expansion**

4/9/15
DIALOG(R)File 2:INSPEC

04194293 INSPEC Abstract Number: B9208-0590-020
Title: Composite **solders**
Author(s): Marshall, J.L.; Calderon, J.; Miiller, D.; DeSimone, M.; Sees, J.; Lucey, G.; Hwang, J.
Author Affiliation: Centre for Mater. Characterization, North Texas Univ., Denton, TX, USA
Conference Title: 1991 Proceedings. 41st Electronic Components and Technology Conference (Cat. No.91CH2989-2) p.647-52
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA xvi+901 pp.
ISBN: 0 7803 0012 2
U.S. Copyright Clearance Center Code: 0569-5503/91/0000-0647$01.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 11-16 May 1991 Conference Location: Atlanta, GA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Development of composite **solders** has been performed utilizing an intermetallic compound interspersed in a **solder** matrix. The principal work has been done on Cu/sub 6/Sn/sub 5/ intermetallic in 60/40 Sn/Pb. The composite **solder** was prepared by mixing powdered intermetallic in **solder** paste, with subsequent reflow. Formulations of 10-40% intermetallic (by weight) were investigated. Optical inspection of cross sections demonstrates that the differentiation of the three phases (Sn, Pb, Cu/sub 6/Sn/sub 5/) is not easy, owing to the similar appearance of Sn and Cu/sub 6/Sn/sub 5/; however, etching with ammonium fluoride/hydrogen peroxide preferentially removes the tin and darkens the lead, making characterization facile. Alternatively, scanning electron micrographs/energy dispersive X-ray (SEM/EDX) analysis of cross sections, using the backscattered detection mode, is an excellent tool for microcharacterization. The mechanical properties of composite **solder** were examined and were found to be superior to those of standard tin/lead **solder**. **Solder** joints were readily prepared utilizing the composite **solder** and were forced to failure by thermocyclic fatigue; the mechanism of failure was the same as for 60/40 Sn/Pb **solder**, i.e., heterogeneous coarsening. (17 Refs)
Subfile: B
Descriptors: fatigue; lead alloys; scanning electron microscope examination of materials; **soldering**; tin alloys; X-ray chemical analysis
Chemical Indexing:
SnPb bin - Pb bin - Sn bin (Elements - 2)
SnPbCu6Sn5 ss - Cu6 ss - Sn5 ss - **Cu ss - Pb ss - Sn ss** (Elements - 3)

4/9/17
DIALOG(R)File 2:INSPEC

04078823 INSPEC Abstract Number: B9203-0530-003
Title: Composite **solders**
Author(s): Marshall, J.L.; Calderon, J.; Sees, J.; Lucey, G.; Hwang, J.S.
Author Affiliation: Center for Mater. Characterization, North Texas Univ., Denton, TX, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.14, no.4 p.698-702
Publication Date: Dec. 1991 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
U.S. Copyright Clearance Center Code: 0148-6411/91/1200-0698$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The characterization of composite **solders** has been performed, specifically on tin/lead/Cu/sub 6/Sn/sub 5/ composition. This characterization includes both microstructural and mechanical analysis. Scanning electron microscope (SEM) characterization of cross sections of the composite **solder** was preferred over optical inspection, owing to the similar appearance of the Sn and Cu/sub 6/Sn/sub 5/ phases by the latter method. The mechanical properties of composites were examined and were found to be superior those of standard tin/lead **solder**. Melting points of composite **solder** were the same as 60/40 tin/lead **solder**. **Solder** joints were readily prepared using the composite **solder** and were forced to failure by thermocyclic fatigue. The mechanism of failure was the same as for 60/40 Sn/Pb **solder**, i.e. heterogeneous coarsening. Auger/ESCA analysis of the intermetallic was performed to ascertain the nature of the surface of this filler, and it was found to be enriched in tin. (24 Refs)
Chemical Indexing:
SnPbCu6Sn5 ss - Cu6 ss - Sn5 ss - **Cu ss** - **Pb ss** - **Sn ss**
(Elements - 3)

4/9/18
DIALOG(R)File 2:INSPEC

04043483 INSPEC Abstract Number: A9202-8130M-004, B9201-0170G-007
Title: eta -Cu/sub 6/Sn/sub 5/ precipitates in Cu/P-Sn **solder** joints
Author(s): Felton, L.E.; Rajan, K.; Ficalora, P.J.
Author Affiliation: Dept. of Mater. Eng., Rensselaer Polytech. Inst., Troy, NY, USA
Journal: Scripta Metallurgica et Materialia vol.25, no.10 p.2329-33
Publication Date: Oct. 1991 Country of Publication: USA
CODEN: SCRMEX ISSN: 0956-716X
U.S. Copyright Clearance Center Code: 0956-716X/91/$3.00
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Reports of the presence of eta -Cu/sub 6/Sn/sub 5/ precipitates in the Sn grains of **solder** joints. During the reflow of the **solder** joint, Cu diffuses through the interfacial eta Cu/sub 6/Sn/sub 5/ layer and dissolves into the molten **solder**. Solidification of the Pb-Sn-Cu alloy produces a solid that is saturated with Cu. Since solubility of Cu in the solid **solder** decreases with temperature, further cooling (for example to room temperature) produces a supersaturation of Cu. The supersaturation can be relieved by the precipitation of eta -Cu/sub 6/Sn/sub 5/. Since the temperature of the **solder** joints is typical of reflows employed in industrial processes, the precipitates are likely generally present in **solder** joints on commercial electronics assemblies. (3 Refs)
Subfile: A B
Descriptors: copper; lead alloys; precipitation; **soldering**; tin
Chemical Indexing:
Cu-PbSn int - PbSn int - Cu int - Pb int - Sn int - PbSn bin - Pb bin - Sn bin - Cu el (Elements - 1,2,3)
Cu6Sn5 bin - Cu6 bin - Sn5 bin - Cu bin - Sn bin (Elements - 2)
PbSnCu ss - **Cu ss** - **Pb ss** - **Sn ss** (Elements - 3)

11/9/18
DIALOG(R)File 2:INSPEC

01445445 INSPEC Abstract Number: B80003359
Title: Circuit package with improved fatigue life
Author(s): Homa, T.R.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.3 p.950
Publication Date: Aug. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: A circuit package has been proposed in which a **flexible** film with appropriate circuit connections is interposed between a circuit chip and a substrate. The **flexible** film is intended to take up the strain caused by the different coefficients of **thermal expansion** of the components in the package. Requirements for the **interconnecting solder** elements are outlined. (0 Refs)
Subfile: B
Descriptors: fatigue; integrated circuit technology; packaging; **soldering**; thermal stress cracking